ISL1571

Power Line Communication (PLC)

The ISL1571 is a dual operational amplifier designed for PLC line driving in Orthogonal Frequency-Division Multiplexing (OFDM) and Spread Spectrum Communication (SSC) based solutions. This device features a high drive capability of 750mA while consuming only 6mA of supply current per amplifier and operating from a single 4.5V to 12V supply. The driver achieves a typical distortion of -80dBc, at 150kHz into a 25Ω load.

The ISL1571 is available in the thermally-enhanced 16 Ld QFN or 10 Ld HMSOP package and is specified for operation across the full -40°C to +85°C temperature range. The ISL1571 has control pins $BIAS_0$ and $BIAS_1$ for controlling the bias and enable/disable of the outputs. These controls allow for lowering the power to fit the performance/power ratio for the application.

The ISL1571 is ideal for line driving applications following the Homeplug 1.0, Homeplug AV and UPA standard based PLC.

Applications

- Homeplug 1.0
- Homeplug AV
- UPA digital home standard

Features

- 21dBm output power capability
- Drives up to 750mA from a +12V supply
- $20V_{P-P}$ differential output drive into 21Ω
- Very low noise floor
- -75dBc typical driver output distortion at 4MHz
- -80dBc typical driver output distortion at 10MHz
- -79dBc typical driver output distortion at 17MHz
- Low quiescent current of 6mA per amplifier
- Supply range
  - ISL1571IUEZ: 4.5V to 12V
  - ISL1571IRZ ±2.25V to ±6V: 4.5V to 12V
- 250MHz bandwidth
- Thermal shutdown
- Pb-free (RoHS compliant)

Related Literature

For a full list of related documents, visit our website:

- ISL1571 device page

1. Overview

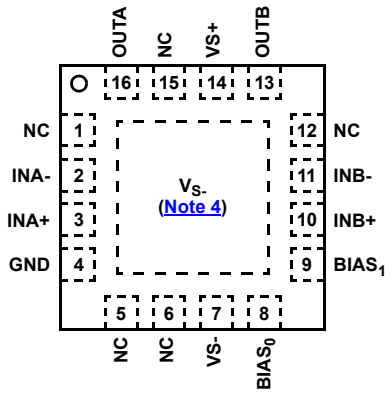
1.1 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL1571IRZ	157 1IRZ	-40 to +85	-	16 Ld QFN	L16.4x4H
ISL1571IRZ-T7	157 1IRZ	-40 to +85	1k	16 Ld QFN	L16.4x4H
ISL1571IUEZ	BBBDA	-40 to +85	-	10 Ld HMSOP	M10.118B
ISL1571IUEZ-T7	BBBDA	-40 to +85	1.5k	10 Ld HMSOP	M10.118B

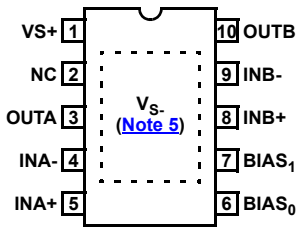
Notes:
1. See TB347 for details on reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL1571 device page. For more information about MSL, see TB363.

1.2 Pin Configuration

16 Ld QFN
Top View



10 Ld HMSOP
Top View



Note:
4. Thermal pad must be connected to negative supply: V_{S-}. QFN package can be used in single and dual supply applications.

Note:
5. Thermal pad must be connected to negative supply: V_{S-}. HMSOP package can be used in single supply applications only.

1.3 Pin Descriptions

16 Ld QFN	10 Ld HMSOP	Pin Name	Function
1, 5, 6, 12, 15	2	NC	No Connect
2	4	INA-	Inverting Input of Amplifier A
3	5	INA+	Non-Inverting Input of Amplifier A
4	Thermal Pad	GND	Ground Connect
7	Thermal Pad	VS-	Negative Supply
8	6	$BIAS_0$ (Note 6)	Current Control Bias Pin
9	7	$BIAS_1$ (Note 6)	Current Control Bias Pin
10	8	INB+	Non-Inverting Input of Amplifier B
11	9	INB-	Inverting Input of Amplifier B
13	10	OUTB	Output of Amplifier B
14	1	VS+	Positive Supply
16	3	OUTA	Output of Amplifier A

Note:
6. The single DSL port is comprised of amplifiers A and B. $BIAS_0$ and $BIAS_1$ control the I_S settings for the DSL port.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_S+ Voltage to Ground	-0.3	+13.2	V
V_{IN}+ Voltage	GND	V_S+	
Current into any Input		8	mA
Continuous Output Current		75	mA
$BIAS_0$, $BIAS_1$ to Ground		+6.6	V
ESD Rating	**Value**		**Unit**
Human Body Model (Note 7)	1		kV
Charge Device Model	1.5		kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:
7. Excludes C0 and C1 pins which show less than 1kV of HBM ESD sensitivity.

2.2 Thermal Information

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature Range	-40	+85	°C
Storage Temperature Range	-60	+150	°C
Operating Junction Temperature		+150	°C
Power Dissipation			See Curves
Pb-Free Reflow Profile	see TB493		

2.3 Electrical Specifications

V_S = 12V, R_F = 750Ω, R_{L-DIFF} = 50Ω, $BIAS_0$ = $BIAS_1$ = 0V, T_A = +25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AC Performance						
-3dB Bandwidth	BW	R_F = 750Ω, A_V = +5		250		MHz
		R_F = 750Ω, A_V = +10		200		MHz
Total Harmonic Distortion, Differential	THD	f = 4MHz, $V_O = 4V_{P-P\_DIFF}$, R_{L-DIFF} = 100Ω		-75		dBc
		f = 10MHz, $V_O = 4V_{P-P\_DIFF}$, R_{L-DIFF} = 100Ω		-80		dBc
		f = 17MHz, $V_O = 4V_{P-P\_DIFF}$, R_{L-DIFF} = 100Ω		-79		dBc
Slew Rate, Single-ended	SR	V_{OUT} from -3V to +3V	750	1200		V/µs
DC Performance						
Offset Voltage Common Mode	V_{OS_CM}		-40		+40	mV
Offset Voltage Differential Mode	V_{OS_DM}		-7.5		+7.5	mV
Differential Transimpedance	R_{OL}	$V_{OUT} = 12V_{P-P}$ differential, unloaded		3.0		MΩ
Input Characteristics						
Non-Inverting Input Bias Current	I_B+		-7.0		+7.0	µA
Inverting Input Bias Current Differential Mode	$I_{B-\ DM}$		-75	3	+75	µA
Input Noise Voltage	e_N			6		$nV\sqrt{Hz}$

V_S = 12V, R_F = 750Ω, $R_{L\text{-}DIFF}$ = 50Ω, $BIAS_0$ = $BIAS_1$ = 0V, T_A = +25°C, unless otherwise specified. **(Continued)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-Input Noise Current	i_N			13		pA/√Hz
Output Characteristics						
Loaded Output Swing (single ended)	V_{OUT}	V_S = ±6V, $R_{L\ DIFF}$ = 50Ω	±4.8	±5.0		V
		V_S = ±6V, $R_{L\ DIFF}$ = 20Ω	±4.35	±4.7		V
Output Current	I_{OUT}	R_L = 0Ω		1000		mA
Supply						
Supply Voltage	V_S	Single supply	4.5		13.2	V
Positive Supply Current per Amplifier	I_S+ (Full Bias)	V_S = 4.5V, no load, $BIAS_0$ = $BIAS_1$ = 0V	12	15	21.5	mA
	I_S+ (Medium Bias)	V_S = 4.5V, no load, $BIAS_0$ = 5V, $BIAS_1$ = 0V		11		mA
	I_S+ (Low Bias)	V_S = 4.5V, no load, $BIAS_0$ = 0V, $BIAS_1$ = 5V		6.0		mA
	I_S+ (Power-down)	V_S = 4.5V, no load, $BIAS_0$ = $BIAS_1$ = 5V		0.6	1.0	mA
$BIAS_0$, $BIAS_1$ Input Current, High	I_{INH}, $BIAS_0$ or $BIAS_1$	$BIAS_0$, $BIAS_1$ = 6V	100	175	250	µA
$BIAS_0$, $BIAS_1$ Input Current, Low	I_{INL}, $BIAS_0$ or $BIAS_1$	$BIAS_0$, $BIAS_1$ = 0V	-5		+5	µA
$BIAS_0$, $BIAS_1$ Input Voltage, High	V_{INH}, $BIAS_0$ or $BIAS_1$		2.0			V
$BIAS_0$, $BIAS_1$ Input Voltage, Low	V_{INL}, $BIAS_0$ or $BIAS_1$				0.8	V

3. Typical Performance Curves

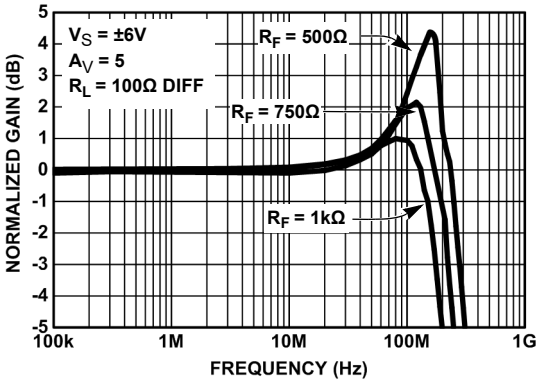


Figure 1. Differential Frequency Response with Various R_F (Full Bias Mode)

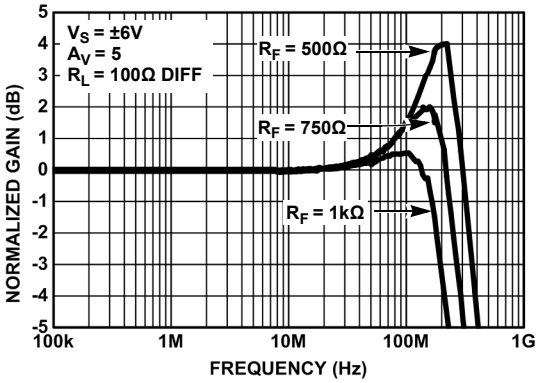


Figure 2. Differential Frequency Response with Various R_F (Medium Bias Mode)

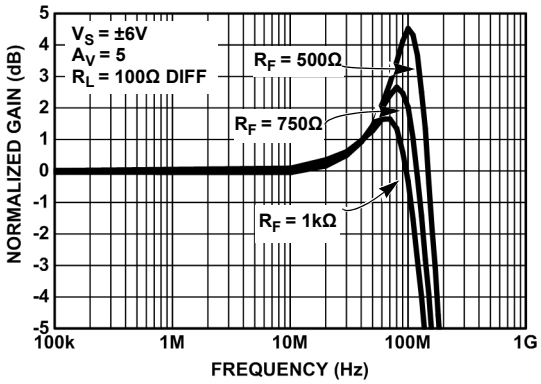


Figure 3. Differential Frequency Response with Various R_F (Low Bias Mode)

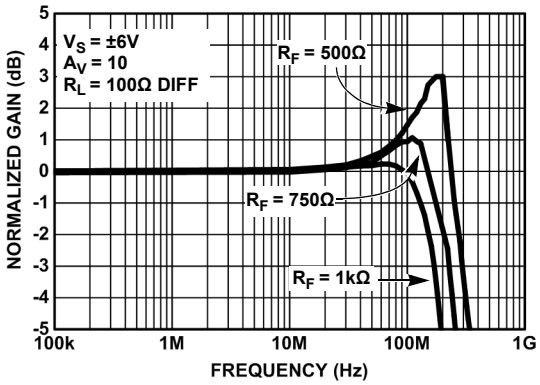


Figure 4. Differential Frequency Response with Various R_F (Full Bias Mode)

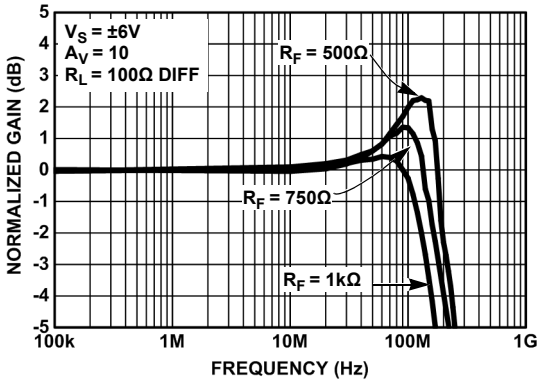


Figure 5. Differential Frequency Response with Various R_F (Medium Bias Mode)

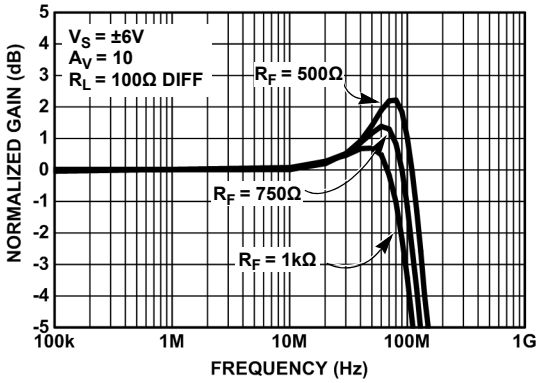


Figure 6. Differential Frequency Response with Various R_F (Low Bias MODE)

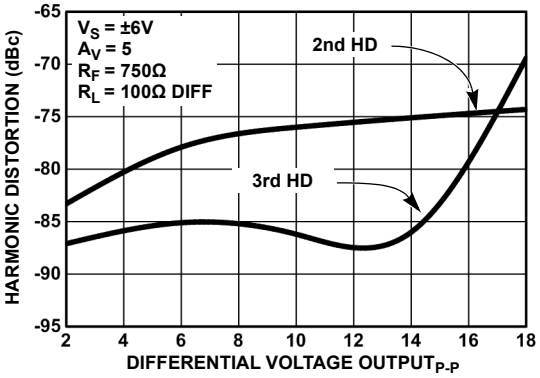


Figure 7. Harmonic Distortion at 2MHz

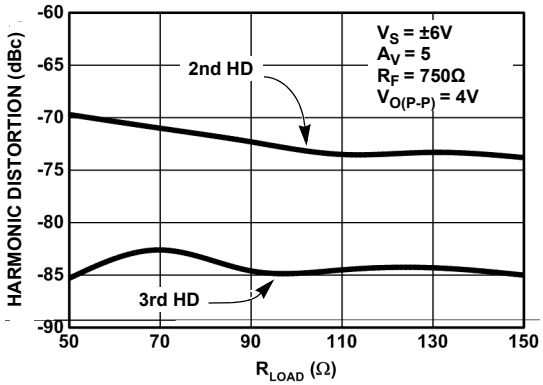


Figure 8. 2nd and 3rd Harmonic Distortion vs R_{LOAD} at 2MHz

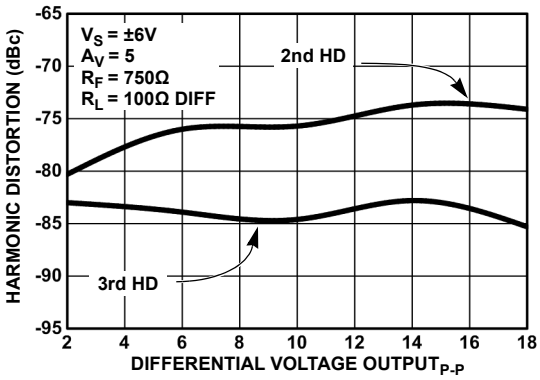


Figure 9. Harmonic Distortion at 3MHz

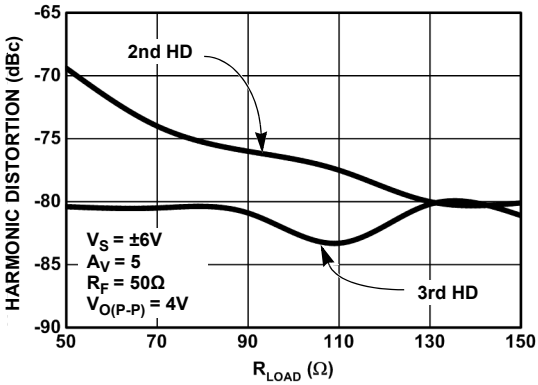


Figure 10. 2nd and 3rd Harmonic Distortion vs R_{LOAD} at 3MHz

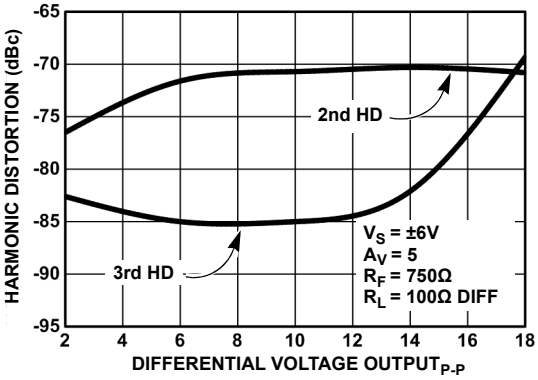


Figure 11. Harmonic Distortion at 5MHz

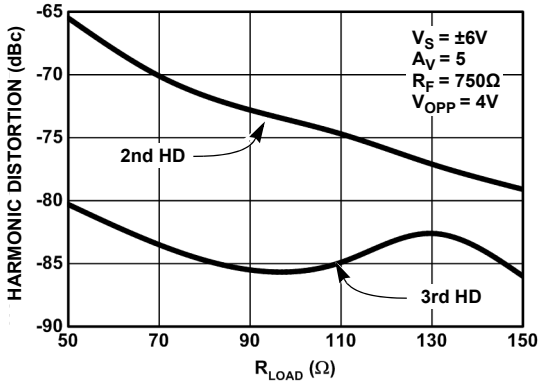


Figure 12. 2nd and 3rd Harmonic Distortion vs R_{LOAD} at 5MHz

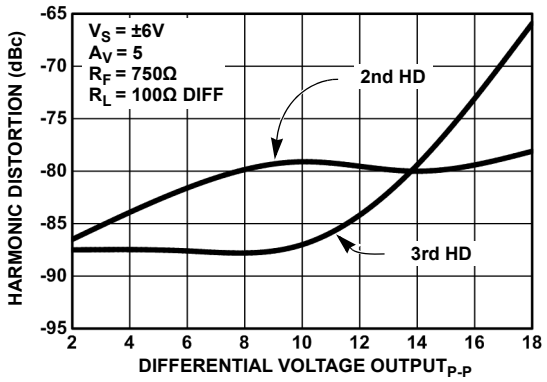


Figure 13. Harmonic Distortion at 10MHz

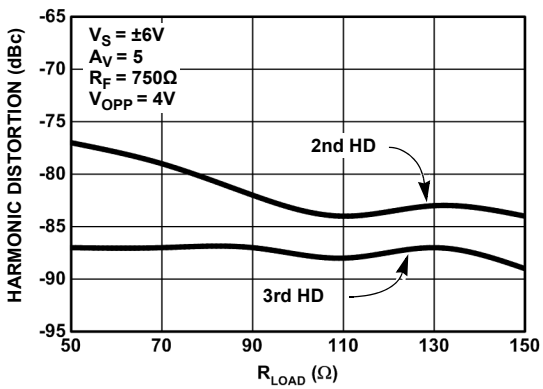


Figure 14. 2nd and 3rd Harmonic Distortion vs R_{LOAD} at 10MHz

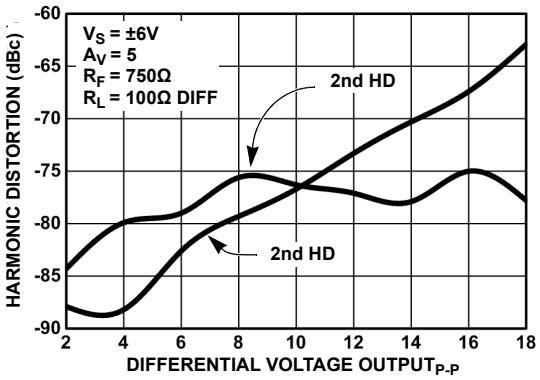


Figure 15. Harmonic Distortion at 17MHz

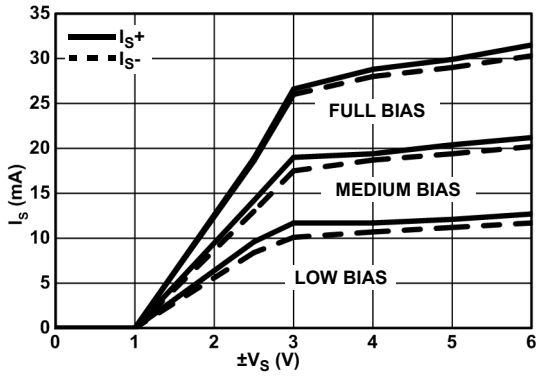


Figure 16. Supply Current vs Supply Voltage

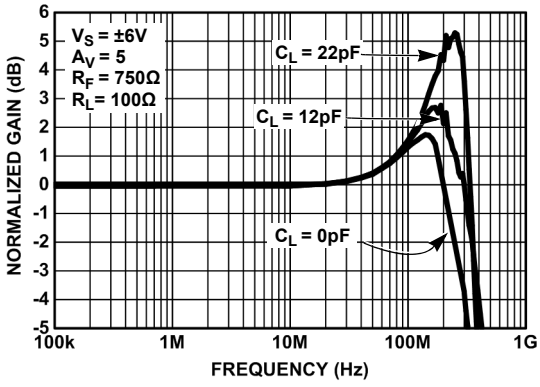


Figure 17. Frequency Response with Various C_L (Full Bias Mode)

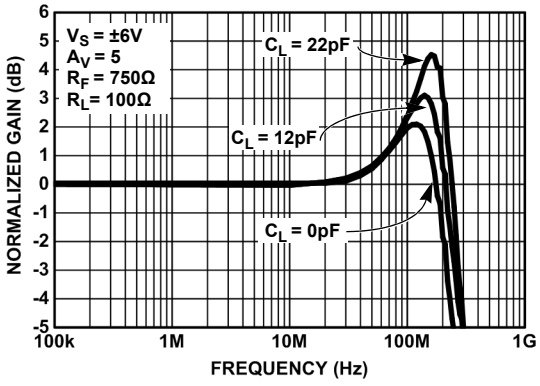


Figure 18. Frequency Response vs Various C_L (Medium Bias Mode)

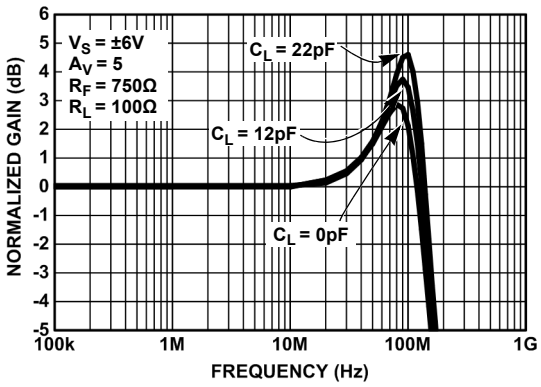


Figure 19. Frequency Response with Various C_L (Low Bias Mode)

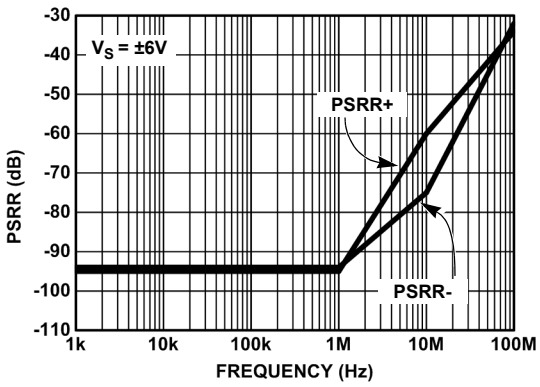


Figure 20. PSRR vs Frequency

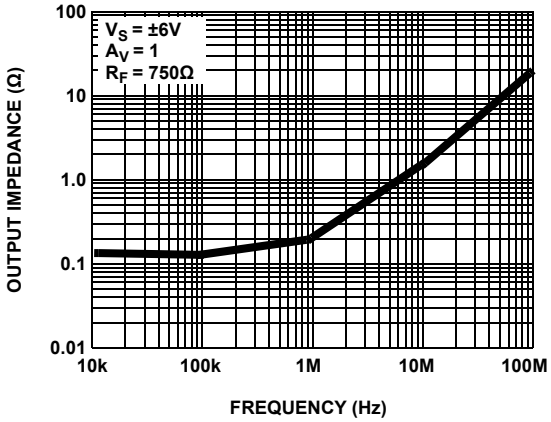


Figure 21. Output Impedance vs Frequency

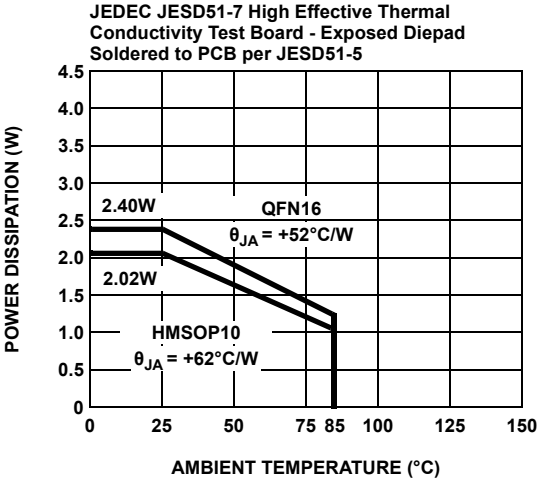


Figure 22. Package Power Dissipation vs Ambient Temperature

4. Product Description

The ISL1571 is a dual operational amplifier designed for line driving in OFDM and PLC solutions. It is a dual current-mode feedback amplifier with low distortion while drawing moderately low supply current. It is built using the Renesas proprietary complimentary bipolar process and is offered in industry standard pin configurations. Due to the current feedback architecture, the ISL1571 closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the "Typical Performance Curves" on page 5, show the effect of varying both R_F and R_G. The 3dB bandwidth is somewhat dependent on the power supply voltage.

4.1 Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below 0.25". The power supply pins must be well bypassed to reduce the risk of oscillation. A 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor is adequate for each supply pin. During power-up, it is necessary to limit the slew rate of the rising power supply to within 1V/µs. If the power supply rising time is undetermined, a series 10Ω resistor on the power supply line can be used to ensure the proper power supply rise time.

For good AC performance, parasitic capacitances is kept to a minimum, especially at the inverting input. This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should be avoided because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

4.2 Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input affects the AC and transient performance of the ISL1571 when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

4.3 Feedback Resistor Values

The ISL1571 has been designed and specified with R_F = 750Ω for A_V = +5. This value of feedback resistor yields extremely flat frequency response with 1dB peaking out to 250MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor causes rolloff to occur at a lower frequency. See the curves in the Typical Performance Curves beginning on page 5, which show 3dB bandwidth and peaking versus frequency for various feedback resistors and various supply voltages.

4.4 Bandwidth vs Temperature

Whereas many amplifier's supply current (and consequently 3dB bandwidth) drop off at high temperature, the ISL1571 was designed to have little supply current variations with temperature. An immediate benefit is the 3dB bandwidth does not drop off drastically with temperature.

4.5 Supply Voltage Range

The ISL1571IRZ has been designed to operate with supply voltages from ±2.25V to ±6V nominal. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages.

4.6 Single Supply Operation

If a single supply is desired, values from +4.5V to +12V nominal can be used as long as the input common-mode range is not exceeded. When using a single supply, be sure to either:

1. DC bias the inputs at an appropriate common-mode voltage and AC couple the signal, or:
2. Ensure the driving signal is within the common-mode range of the ISL1571. ISL1571IUEZ must be used in single supply applications.

4.7 PLC Modem Applications

The ISL1571 is designed as a line driver for PLC modems. It is capable of outputting 450mA of output current with a typical supply voltage headroom of 1.3V. It can achieve -85dBc of distortion at low 7.1mA of supply current per amplifier.

The average line power requirement for the PLC application is 13dBm (20mW) into a 100Ω line. The average line voltage is $1.41V_{RMS}$. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:2 is selected. The circuit configuration is shown in Figure 23.

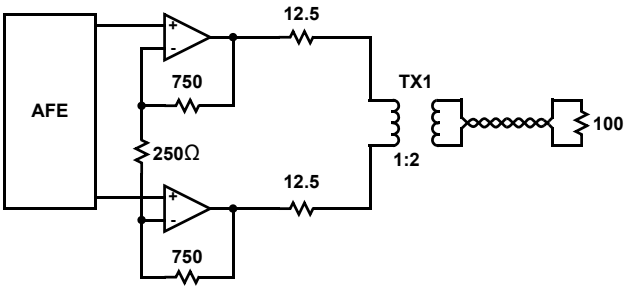


Figure 23. Circuit Configuration

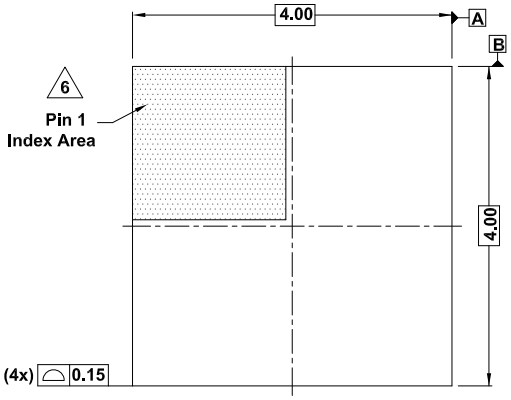
5. Revision History

Rev.	Date	Description
4.00	Jul.17.20	Updated POD L16.4x4H to the latest revision, changes are as follows: -Added note 7 and the Note 7 references to bottom view and Typ Pattern view -Removed “base plane” from side view -Updated the lead width dimension from 0.33 ±0.02 to 0.33 ±0.05
3.00	Nov.7.19	Changed POD MDP0050 to POD M10.118B in the ordering information table and in the Package Outline Drawings section.
2.00	Jun.14.19	Applied new formatting throughout. Updated Ordering Information table: Added Tape and Reel quantity column, added MSL note Electrical Specifications table, Supply section: Positive Supply Current per Amplifier, Test Conditions - added “V_S = 4.5V, no load,” POD MDP0046: Replaced POD MDP0046 with L16.4x4H. Updated disclaimer.

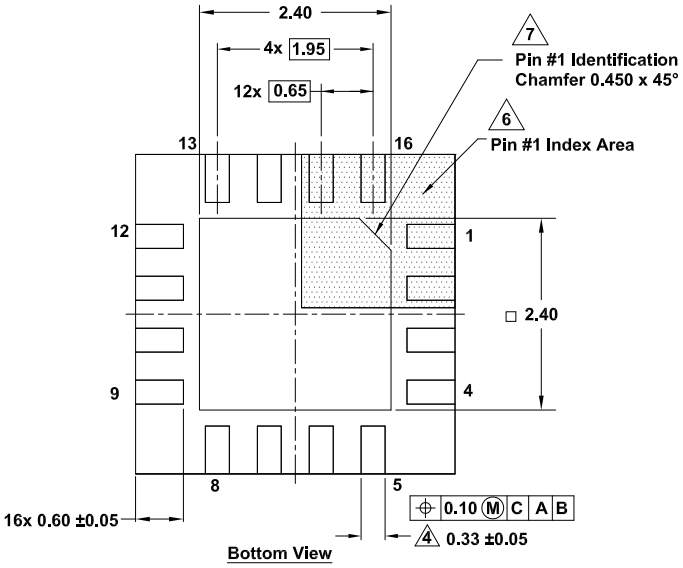
6. Package Outline Drawings

For the most recent package outline drawing, see L16.4x4H.

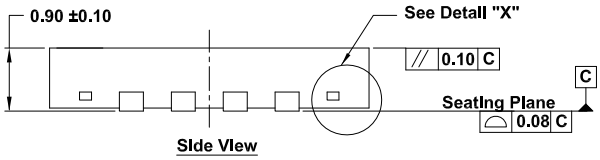
L16.4x4H
16 Lead Quad Flat No-Lead Plastic Package
Rev 1, 7/20



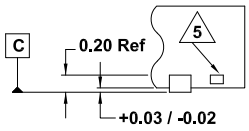
Top View



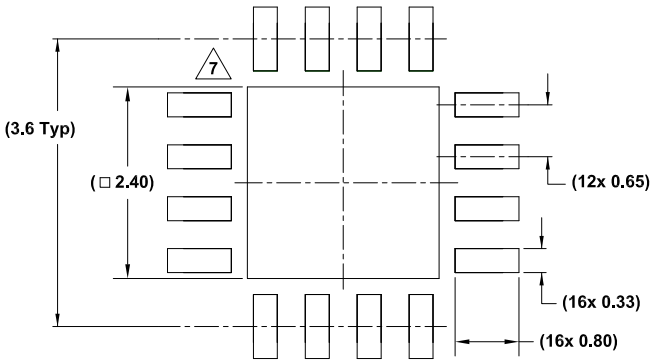
Bottom View



Side View



Detail "X"

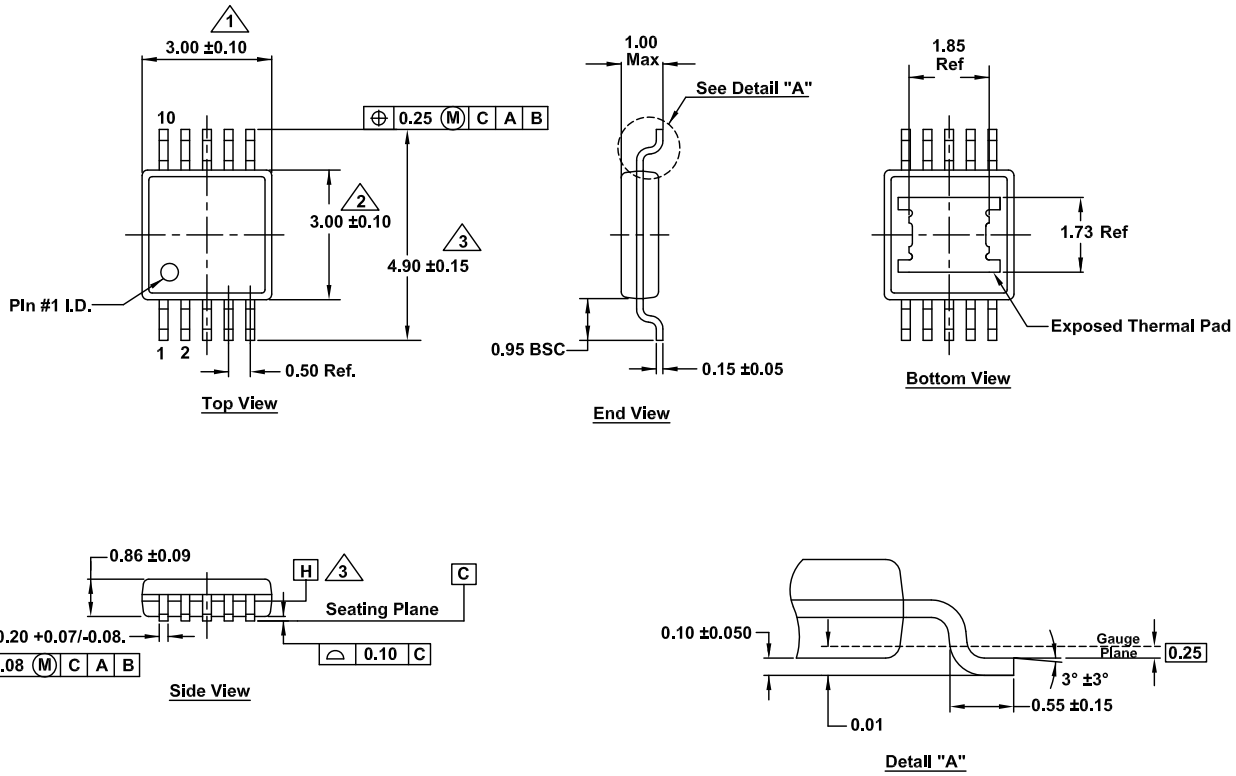


Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.
7. Pin 1 corner chamfer not required.

M10.118B For the most recent package outline drawing, see M10.118B.
10 Lead Heatsink Mini Small Outline Plastic Package (HMSOP, Heatsink MSOP)
Rev 2, 10/19



Notes:

1. Plastic or metal protrusions of 0.15 maximum per side are not included.
2. Plastic interlead protrusions of 0.25 maximum per side are not included.
3. Package body length and width dimensions are measured at Datum Plane "H".
4. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
5. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.