128 Mb/256 Mb/512 Mb/1 Gb GL-S MIRRORBIT™ Flash

Parallel, 3.0 V

General description

The S29GL01G/512/256/128S are MIRRORBIT™ Eclipse flash products fabricated on 65-nm process technology. These devices offer a fast page access time as fast as 15 ns with a corresponding random access time as fast as 90 ns. They feature a Write Buffer that allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes these devices ideal for today's embedded applications that require higher density, better performance and lower power consumption.

Distinctive characteristics

- CMOS 3.0 V core with versatile I/O
- 65 nm MIRRORBIT™ Eclipse technology
- Single supply (V_{CC}) for read / program / erase (2.7 V to 3.6 V)
- Versatile I/O feature
  - Wide I/O voltage range (V_{IO}): 1.65 V to V_{CC}
- ×16 data bus
- Asynchronous 32-byte page read
- 512-byte programming buffer
  - Programming in page multiples, up to a maximum of 512 bytes
- Single word and multiple program on same word options
- Automatic error checking and correction (ECC) – internal hardware ECC with single bit error correction
- Sector erase
  - Uniform 128-kbyte sectors
- Suspend and resume commands for program and erase operations
- Status register, data polling, and ready/busy pin methods to determine device status
- Advanced sector protection (ASP)
  - Volatile and non-volatile protection methods for each sector
- Separate 1024-byte one time program (OTP) array with two lockable regions
- Common flash interface (CFI) parameter table
- Temperature range / grade
  - Industrial (–40°C to +85°C)
  - Industrial plus(–40°C to +105°C)
  - Automotive, AEC-Q100 grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 grade 2 (–40°C to +105°C)
- 100,000 program / erase cycles
- 20 years data retention

- Packaging options
  - 56-pin TSOP
  - 64-ball LAA Fortified BGA, 13 mm × 11 mm
  - 64-ball LAE Fortified BGA, 9 mm × 9 mm
  - 56-ball VBU Fortified BGA, 9 mm × 7 mm

Performance summary

Maximum read access times

Density	Voltage range	Random access time (t_{ACC})	Page access time (t_{PACC})	CE# access time (t_{CE})	OE# access time (t_{OE})
128 Mb	Full V_{CC} = V_{IO}	90	15	90	25
	VersatileIO V_{IO}	100	25	100	35
256 Mb	Full V_{CC} = V_{IO}	90	15	90	25
	VersatileIO V_{IO}	100	25	100	35
512 Mb	Full V_{CC} = V_{IO}	100	15	100	25
	VersatileIO V_{IO}	110	25	110	35
1 Gb	Full V_{CC} = V_{IO}	100	15	100	25
	VersatileIO V_{IO}	110	25	110	35

Typical program and erase rates

Operation	Rates
Buffer programming (512 bytes)	1.5 MBps
Sector erase (128 kbytes)	477 kBps

Maximum current consumption

Operation	Unit
Active read at 5 MHz, 30 pF	60 mA
Program	100 mA
Erase	100 mA
Standby	100 µA

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1 Product overview

The GL-S family consists of 128-Mb to 1-Gb, 3.0 V core, versatile I/O, non-volatile, flash memory devices. These devices have a 16-bit (word) wide data bus and use only word boundary addresses. All read accesses provide 16 bits of data on each bus transfer cycle. All writes take 16 bits of data from each bus transfer cycle.

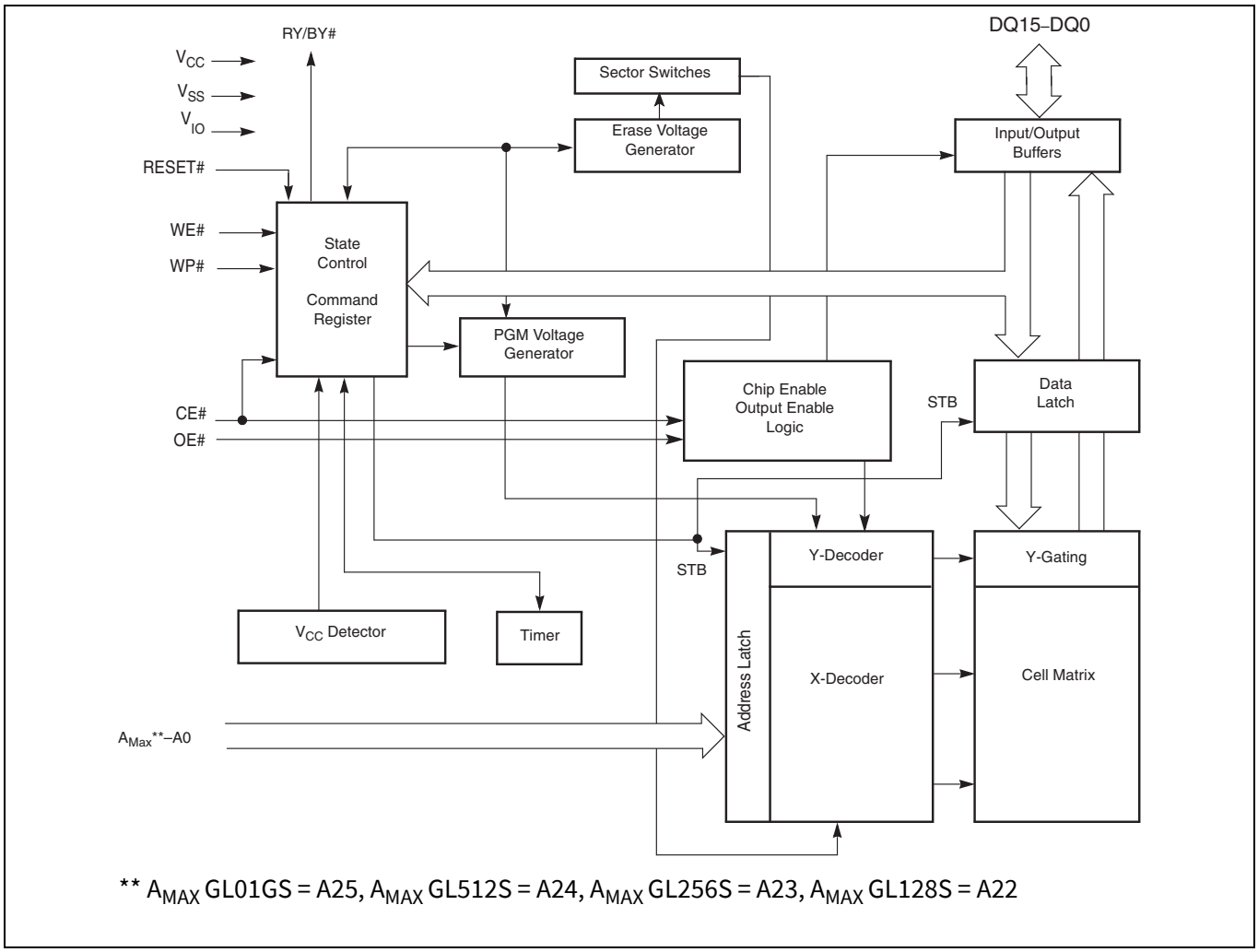


Figure 1 Block diagram

The GL-S family combines the best features of eXecute-In-Place (XIP) and data storage flash memories. This family has the fast random access of XIP flash along with the high density and fast program speed of Data Storage flash.

Read access to any random location takes 90 ns to 120 ns depending on device density and I/O power supply voltage. Each random (initial) access reads an entire 32-byte aligned group of data called a page. Other words within the same page may be read by changing only the low order 4 bits of word address. Each access within the same page takes 15 ns to 30 ns. This is called page mode read. Changing any of the higher word address bits will select a different page and begin a new initial access. All read accesses are asynchronous.

Table 1 S29GL-S address map

Type	Count	Addresses
Address within page	16	A3–A0
Address within write buffer	256	A7–A0
Page	4096	A15–A4
Write-buffer-line	256	A15–A8
Sector	1024 (1 Gb) 512 (512 Mb) 256 (256 Mb) 128 (128 Mb)	A_{MAX}–A16

The device control logic is subdivided into two parallel operating sections, the host interface controller (HIC) and the embedded algorithm controller (EAC). HIC monitors signal levels on the device inputs and drives outputs as needed to complete read and write data transfers with the host system. HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory; notifies the EAC of power transition, hardware reset, and write transfers. The EAC looks in the command memory, after a write transfer, for legal command sequences and performs the related embedded algorithms.

Changing the non-volatile data in the memory array requires a complex sequence of operations that are called embedded algorithms (EA). The algorithms are managed entirely by the device internal EAC. The main algorithms perform programming and erase of the main array data. The host system writes command codes to the flash device address space. The EAC receives the commands, performs all the necessary steps to complete the command, and provides status information during the progress of an EA.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (High) to a logic 0 (Low). Only an Erase operation is able to change ‘0’ to ‘1’. An erase operation must be performed on an entire 128-kbyte aligned and length group of data call a sector. When shipped from Infineon all sectors are erased.

Programming is done via a 512-byte write buffer. It is possible to write from 1 to 256 words, anywhere within the write buffer before starting a programming operation. Within the flash memory array, each 512-byte aligned group of 512 bytes is called a line. A programming operation transfers volatile data from the write buffer to a non-volatile memory array line. The operation is called write buffer programming.

As the device transfers each 32-byte aligned page of data that was loaded into the write buffer to the 512-byte flash array line, internal logic programs an ECC Code for the Page into a portion of the memory array not visible to the host system software. The internal logic checks the ECC information during the initial access of every array read operation. If needed, the ECC information corrects a one bit error during the initial access time.

The write buffer is filled with 1’s after reset or the completion of any operation using the write buffer. Any locations not written to a ‘0’ by a Write to Buffer command are by default still filled with 1’s. Any 1’s in the write buffer do not affect data in the memory array during a programming operation.

As each page of data that was loaded into the write buffer is transferred to a memory array line.

Sectors may be individually protected from program and erase operations by the advanced sector protection (ASP) feature set. ASP provides several, hardware and software controlled, volatile and non-volatile, methods to select which sectors are protected from program and erase operations.

2 Address space maps

There are several separate address spaces that may appear within the address range of the flash memory device. One address space is visible (entered) at any given time.

- Flash memory array: the main non-volatile memory array used for storage of data that may be randomly accessed by asynchronous read operations.
- ID/CFI: a memory array used for Infineon factory programmed device characteristics information. This area contains the device identification (ID) and common flash interface (CFI) information tables.
- Secure silicon region (SSR): a one time programmable (OTP) non-volatile memory array used for Infineon factory programmed permanent data, and customer programmable permanent data.
- Lock register: an OTP non-volatile word used to configure the ASP features and lock the SSR.
- Persistent protection bits (PPB): a non-volatile flash memory array with one bit for each sector. When programmed, each bit protects the related sector from erasure and programming.
- PPB lock: a volatile register bit used to enable or disable programming and erasure of the PPB bits.
- Password: an OTP non-volatile array used to store a 64-bit password used to enable changing the state of the PPB lock bit when using password mode sector protection.
- Dynamic protection bits (DYB): a volatile array with one bit for each sector. When set, each bit protects the related sector from erasure and programming.
- Status register: a volatile register used to display embedded algorithm status.
- Data polling status: a volatile register used as an alternate, legacy software compatible, way to display embedded algorithm status.
- ECC status: provides the status of any error detection or correction action taken when reading the selected page.

The main flash memory array is the primary and default address space but, it may be overlaid by one other address space, at any one time. Each alternate address space is called an address space overlay (ASO).

Each ASO replaces (overlays) the entire flash device address range. Any address range not defined by a particular ASO address map, is reserved for future use. All read accesses outside of an ASO address map returns non-valid (undefined) data. The locations will display actively driven data but the meaning of whatever 1's or 0's appear are not defined.

There are four device operating modes that determine what appears in the flash device address space at any given time:

- Read mode
- Data polling mode
- Status register (SR) mode
- Address space overlay (ASO) mode

In read mode the entire flash memory array may be directly read by the host system memory controller. The memory device embedded algorithm controller (EAC), puts the device in read mode during power-on, after a hardware reset, after a command reset, or after an embedded algorithm (EA) is suspended. Read accesses and command writes are accepted in read mode. A subset of commands are accepted in read mode when an EA is suspended.

While in any mode, the status register read command may be issued to cause the status register ASO to appear at every word address in the device address space. In this status register ASO Mode, the device interface waits for a read access and, any write access is ignored. The next read access to the device accesses the content of the status register, exits the status register ASO, and returns to the previous (calling) mode in which the status register read command was received.

In EA mode the EAC is performing an embedded algorithm, such as programming or erasing a non-volatile memory array. While in EA mode, none of the main flash memory array is readable because the entire flash device address space is replaced by the data polling status ASO. Data Polling Status will appear at every word location in the device address space.

While in EA mode, only a program / erase suspend command or the status register read command will be accepted. All other commands are ignored. Thus, no other ASO may be entered from the EA mode.

When an embedded algorithm is suspended, the data polling ASO is visible until the device has suspended the EA. When the EA is suspended the data polling ASO is exited and flash array data is available. The data polling ASO is reentered when the suspended EA is resumed, until the EA is again suspended or finished. When an embedded algorithm is completed, the data polling ASO is exited and the device goes to the previous (calling) mode (from which the embedded algorithm was started).

In ASO mode, one of the remaining overlay address spaces is entered (overlaid on the main flash Array address map). Only one ASO may be entered at any one time. Commands to the device affect the currently entered ASO. Only certain commands are valid for each ASO. These are listed in the **Table 41**, in each ASO related section of the table.

The following ASOs have non-volatile data that may be programmed to change 1's to 0's:

- Secure silicon region
- Lock register
- Persistent protection bits (PPB)
- Password
- Only the PPB ASO has non-volatile data that may be erased to change 0's to 1's

When a program or erase command is issued while one of the non-volatile ASOs is entered, the EA operates on the ASO. The ASO is not readable while the EA is active. When the EA is completed the ASO remains entered and is again readable. Suspend and Resume commands are ignored during an EA operating on any of these ASOs.

2.1 Flash memory array

The S29GL-S family has uniform sector architecture with a sector size of 128 kB. **Table 2** to **Table 5** shows the sector architecture of the four devices.

Table 2 S29GL01GS sector and memory address map

Sector size (kbyte)	Sector count	Sector range	Address range (16-bit)	Notes
128	1024	SA00	0000000h–000FFFFh	Sector starting address
		:	:	–
		SA1023	3FF0000h–3FFFFFFh	Sector ending address

Table 3 S29GL512S sector and memory address map

Sector size (kbyte)	Sector count	Sector range	Address range (16-bit)	Notes
128	512	SA00	0000000h–000FFFFh	Sector starting address
		:	:	–
		SA511	1FF0000h–1FFFFFFh	Sector ending address

Table 4 S29GL256S sector and memory address map

Sector size (kbyte)	Sector count	Sector range	Address range (16-bit)	Notes
128	256	SA00	0000000h–000FFFFh	Sector starting address
		:	:	–
		SA255	0FF0000h–0FFFFFFh	Sector ending address

Table 5 S29GL128S sector and memory address map

Sector size (kbyte)	Sector count	Sector range	Address range (16-bit)	Notes
128	128	SA00	0000000h–000FFFFh	Sector starting address
		:	:	–
		SA127	07F0000h–07FFFFFh	Sector ending address

Note: These tables have been condensed to show sector related information for an entire device on a single page Sectors and their address ranges that are not explicitly listed (such as SA001–SA510) have sectors starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 kB sectors have the pattern XXX0000h–XXXFFFFh.

2.2 Device ID and CFI (ID-CFI) ASO

There are two traditional methods for systems to identify the type of flash memory installed in the system. One has traditionally been called Autoselect and is now referred to as device identification (ID). The other method is called common flash interface (CFI).

For ID, a command is used to enable an address space overlay where up to 16 word locations can be read to get JEDEC manufacturer identification (ID), device ID, and some configuration and protection status information from the flash memory. The system can use the manufacturer and device IDs to select the appropriate driver software to use with the flash device.

CFI also uses a command to enable an address space overlay where an extendable table of standard information about how the flash memory is organized and operates can be read. With this method the driver software does not have to be written with the specifics of each possible memory device in mind. Instead the driver software is written in a more general way to handle many different devices but adjusts the driver behavior based on the information in the CFI table.

Traditionally these two address spaces have used separate commands and were separate overlays. However, the mapping of these two address spaces are non-overlapping and so can be combined in to a single address space and appear together in a single overlay. Either of the traditional commands used to access (enter) the autoselect (ID) or CFI overlay will cause the now combined ID-CFI address map to appear.

The ID-CFI address map appears within, and overlays the flash array data of, the sector selected by the address used in the ID-CFI enter command. While the ID-CFI ASO is entered the content of all other sectors is undefined.

The ID-CFI address map starts at location '0' of the selected sector. Locations above the maximum defined address of the ID-CFI ASO to the maximum address of the selected sector have undefined data. The ID-CFI enter commands use the same address and data values used on previous generation memories to access the JEDEC Manufacturer ID (Autoselect) and common flash interface (CFI) information, respectively. See **Figure 28** for ASO Entry timing requirements.

Table 6 ID-CFI address map overview

Word address	Description	Read / Write
(SA) + 0000h to 000Fh	Device ID (traditional Autoselect values)	Read only
(SA) + 0010h to 0079h	CFI data structure	Read only
(SA) + 0080h to FFFFh	Undefined	Read only

For the complete address map see **Table 42**.

2.3 Device ID and common flash interface (ID-CFI) ASO map — automotive only

Table 7 Device ID and common flash interface (ID-CFI) ASO map — automotive only

Word address	Data field	# of bytes	Data format	Example of actual data	Hex read out of example data
(SA) + 0080h	Size of Electronic Marking	1	Hex	19	0013h
(SA) + 0081h	Revision of Electronic Marking	1	Hex	1	0001h
(SA) + 0082h	Fab Lot #	7	Ascii	LD87270	004Ch, 0044h, 0038h, 0037h, 0032h, 0037h, 0030h
(SA) + 0089h	Wafer #	1	Hex	23	0017h
(SA) + 008Ah	Die X coordinate	1	Hex	10	000Ah
(SA) + 008Bh	Die Y coordinate	1	Hex	15	000Fh
(SA) + 008Ch	Class Lot #	7	Ascii	BR33150	0042h, 0052h, 0033h, 0033h, 0031h, 0035h, 0030h
(SA) + 0093h	Reserved for future	13	n/a	n/a	undefined

Fab Lot # + Wafer # + Die X coordinate + Die Y coordinate gives a unique ID for each device.

2.3.1 Device ID

The Joint Electron Device Engineering Council (JEDEC) standard JEP106T defines the manufacturer ID for a compliant memory. Common industry usage defined a method and format for reading the manufacturer ID and a device specific ID from a memory device. The manufacturer and device ID information is primarily intended for programming equipment to automatically match a device with the corresponding programming algorithm. Infineon has added additional fields within this 32-byte address space.

The original industry format was structured to work with any memory data bus width e. g. ×8, ×16, ×32. The ID code values are traditionally byte wide but are located at bus width address boundaries such that incrementing the device address inputs will read successive byte, word, or double word locations with the ID codes always located in the least significant byte location of the data bus. Because the device data bus is word wide each code byte is located in the lower half of each word location. The original industry format made the high order byte always '0'. Infineon has modified the format to use both bytes in some words of the address space. For the detail description of the device ID address map see **Table 42**.

2.3.2 Common flash memory interface

The JEDEC common flash interface (CFI) specification (JESD68.01) defines a standardized data structure that may be read from a flash memory device, which allows vendor-specified software algorithms to be used for entire families of devices. The data structure contains information for system configuration such as various electrical and timing parameters, and special functions supported by the device. Software support can then be device-independent, device ID-independent, and forward-and-backward-compatible for entire flash device families.

The system can read CFI information at the addresses within the selected sector as shown in **"Device ID and Common Flash Interface (ID-CFI) ASO Map"** on page 61.

Like the device ID information, CFI information is structured to work with any memory data bus width e. g. ×8, ×16, ×32. The code values are always byte wide but are located at data bus width address boundaries such that incrementing the device address reads successive byte, word, or double word locations with the codes always located in the least significant byte location of the data bus. Because the data bus is word wide each code byte is located in the lower half of each word location and the high order byte is always '0'.

For further information, please refer to the *Infineon CFI Specification, Version 1.4* (or later), and the *JEDEC publications JEP137-A and JESD68.01*. Contact JEDEC (**www.jedec.org**) for their standards.

2.4 Status register ASO

The status register ASO contains a single word of registered volatile status for embedded algorithms. When the status register read command is issued, the current status is captured (by the rising edge of WE#) into the register and the ASO is entered. The status register content appears on all word locations. The first read access exits the status register ASO (with the rising edge of CE# or OE#) and returns to the address space map in use when the status register read command was issued. Write commands will not exit the status register ASO state.

2.5 Data polling status ASO

The data polling status ASO contains a single word of volatile memory indicating the progress of an EA. The data polling status ASO is entered immediately following the last write cycle of any command sequence that initiates an EA. Commands that initiate an EA are:

- Word program
- Program buffer to flash
- Chip erase
- Sector erase
- Erase resume / program resume
- Program resume enhanced method
- Blank check
- Lock register program
- Password program
- PPB program
- All PPB erase

Engineering Note: The reset and write buffer abort reset commands require very short time to execute so data polling is not supported for these commands. The data polling status word appears at all word locations in the device address space. When an EA is completed the data polling status ASO is exited and the device address space returns to the address map mode where the EA was started.

2.6 Secure silicon region ASO

The secure silicon region (SSR) provides an extra flash memory area that can be programmed once and permanently protected from further changes i. e. it is a one time program (OTP) area. The SSR is 1024 bytes in length. It consists of 512 bytes for factory locked secure silicon region and 512 bytes for customer locked secure silicon region.

The sector address supplied during the secure silicon entry command selects the flash memory array sector that is overlaid by the secure silicon region address map. See **Figure 28** for ASO entry timing requirements. The SSR is overlaid starting at location 0 in the selected sector. Use of the sector 0 address is recommended for future compatibility. While the SSR ASO is entered the content of all other sectors is undefined. Locations above the maximum defined address of the SSR ASO to the maximum address of the selected sector have undefined data.

Table 8 Secure silicon region

Word address range	Content	Size
(SA) + 0000h to 00FFh	Factory locked secure silicon region	512 bytes
(SA) + 0100h to 01FFh	Customer locked secure silicon region	512 bytes
(SA) + 0200h to FFFFh	Undefined	127 kbytes

2.7 Sector protection control

2.7.1 Lock register ASO

The lock register ASO contains a single word of OTP memory. When the ASO is entered the lock register appears at all word locations in the device address space. See **Figure 28** for ASO Entry timing requirements. However, it is recommended to read or program the lock register only at location 0 of the device address space for future compatibility.

2.7.2 Persistent protection bits (PPB) ASO

The PPB ASO contains one bit of a flash memory array for each Sector in the device. When the PPB ASO is entered, the PPB bit for a sector appears in the least significant bit (LSB) of each address in the sector. See **Figure 28** for ASO Entry timing requirements. Reading any address in a sector displays data where the LSB indicates the non-volatile protection status for that sector. However, it is recommended to read or program the PPB only at address ‘0’ of the sector for future compatibility. If the bit is ‘0’, the sector is protected against programming and erase operations. If the bit is ‘1’, the sector is not protected by the PPB. The sector may be protected by other features of ASP.

2.7.3 PPB LOCK ASO

The PPB lock ASO contains a single bit of volatile memory. The bit controls whether the bits in the PPB ASO may be programmed or erased. If the bit is ‘0’, the PPB ASO is protected against programming and erase operations. If the bit is ‘1’, the PPB ASO is not protected. When the PPB Lock ASO is entered the PPB Lock bit appears in the least significant bit (LSB) of each address in the device address space. See **Figure 28** for ASO Entry timing requirements. However, it is recommended to read or program the PPB Lock only at address 0 of the device for future compatibility.

2.7.4 Password ASO

The password ASO contains four words of OTP memory. When the ASO is entered the password appears starting at address 0 in the device address space. See **Figure 28** for ASO Entry timing requirements. All locations above the forth word are undefined.

2.7.5 Dynamic protection bits (DYB) ASO

The DYB ASO contains one bit of a volatile memory array for each Sector in the device. When the DYB ASO is entered, the DYB bit for a sector appears in the Least Significant Bit (LSB) of each address in the sector. See **Figure 28** for ASO entry timing requirements. Reading any address in a sector displays data where the LSB indicates the non-volatile protection status for that sector. However, it is recommended to read, set, or clear the DYB only at address 0 of the sector for future compatibility. If the bit is '0', the sector is protected against programming and erase operations. If the bit is '1', the sector is not protected by the DYB. The sector may be protected by other features of ASP.

2.8 ECC status ASO

The system can access the ECC status ASO by issuing the ECC status entry command sequence during read mode. The ECC status ASO provides the status of a single bit error correction when reading the selected page. **"Automatic ECC"** on page 23 describes the ECC function in more detail. See **Figure 28** for ASO Entry timing requirements.

The ECC Status ASO allows the following activities:

- Read ECC Status for the selected page.
- ASO exit.

2.8.1 ECC status

The contents of the ECC Status ASO indicates, for the selected ECC page, whether ECC protection has corrected an error in the eight-bit error correction code or the 16 Words of data in the ECC page. The address specified in the ECC Status Read Command, provided in **Table 41** selects the ECC Page.

Table 9 ECC status word – upper byte

Bit	15	14	13	12	11	10	9	8
Name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Value	X	X	X	X	X	X	X	X

Table 10 ECC status word – lower byte

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	RFU	Single bit error corrected in the 8-bit error correction code	Single bit error corrected in 16 words of data	RFU
Value	X	X	X	X	X	0 = No error corrected 1 = Single bit error corrected	0 = No error corrected 1 = Single bit error corrected	X

3 Data protection

The device offers several features to prevent malicious or accidental modification of any sector via hardware means.

3.1 Device protection methods

3.1.1 Power-up write inhibit

RESET#, CE#, WE#, and, OE# are ignored during power-on reset (POR). During POR, the device can not be selected, will not accept commands on the rising edge of WE#, and does not drive outputs. The host interface controller (HIC) and embedded algorithm controller (EAC) are reset to their standby states, ready for reading array data, during POR. CE# or OE# must go to V_{IH} before the end of POR (t_{VCS}).

At the end of POR the device conditions are:

- all internal configuration information is loaded,
- the device is in read mode,
- the status register is at default value,
- all bits in the DYB ASO are set to un-protect all sectors,
- the write buffer is loaded with all 1's,
- the EAC is in the standby state.

3.1.2 Low V_{CC} write inhibit

When V_{CC} is less than V_{LKO}, the HIC does not accept any write cycles and the EAC resets. This protects data during V_{CC} power-up and power-down. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

3.2 Command protection

Embedded algorithms are initiated by writing command sequences into the EAC command memory. The command memory array is not readable by the host system and has no ASO. Each host interface write is a command or part of a command sequence to the device. The EAC examines the address and data in each write transfer to determine if the write is part of a legal command sequence. When a legal command sequence is complete the EAC will initiate the appropriate EA.

Writing incorrect address or data values, or writing them in an improper sequence, will generally result in the EAC returning to its standby state. However, such an improper command sequence may place the device in an unknown state, in which case the system must write the reset command, or possibly provide a hardware reset by driving the RESET# signal LOW, to return the EAC to its Standby state, ready for random read.

The address provided in each write may contain a bit pattern used to help identify the write as a command to the device. The upper portion of the address may also select the sector address on which the command operation is to be performed. The sector address (SA) includes A_{MAX} through A16 flash address bits (system byte address signals a_{max} through a17). A command bit pattern is located in A10 to A0 flash address bits (system byte address signals a11 through a1).

The data in each write may be: a bit pattern used to help identify the write as a command, a code that identifies the command operation to be performed, or supply information needed to perform the operation. See **Table 41** for a listing of all commands accepted by the device.

3.3 Secure silicon region (OTP)

The secure silicon region (SSR) provides an extra flash memory area that can be programmed once and permanently protected from further changes i. e. it is a one time program (OTP) area. The SSR is 1024 bytes in length. It consists of 512 bytes for factory locked secure silicon region and 512 bytes for customer locked secure silicon region.

3.4 Sector protection methods

3.4.1 Write protect signal

If WP# = V_{IL}, the lowest or highest address sector is protected from program or erase operations independent of any other ASP configuration. Whether it is the lowest or highest sector depends on the device ordering option (model) selected. If WP# = V_{IH}, the lowest or highest address sector is not protected by the WP# signal but it may be protected by other aspects of ASP configuration. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}.

3.4.2 ASP

Advanced sector protection (ASP) is a set of independent hardware and software methods used to disable or enable programming or erase operations, individually, in any or all sectors. This section describes the various methods of protecting data stored in the memory array. An overview of these methods is shown in **Figure 2**.

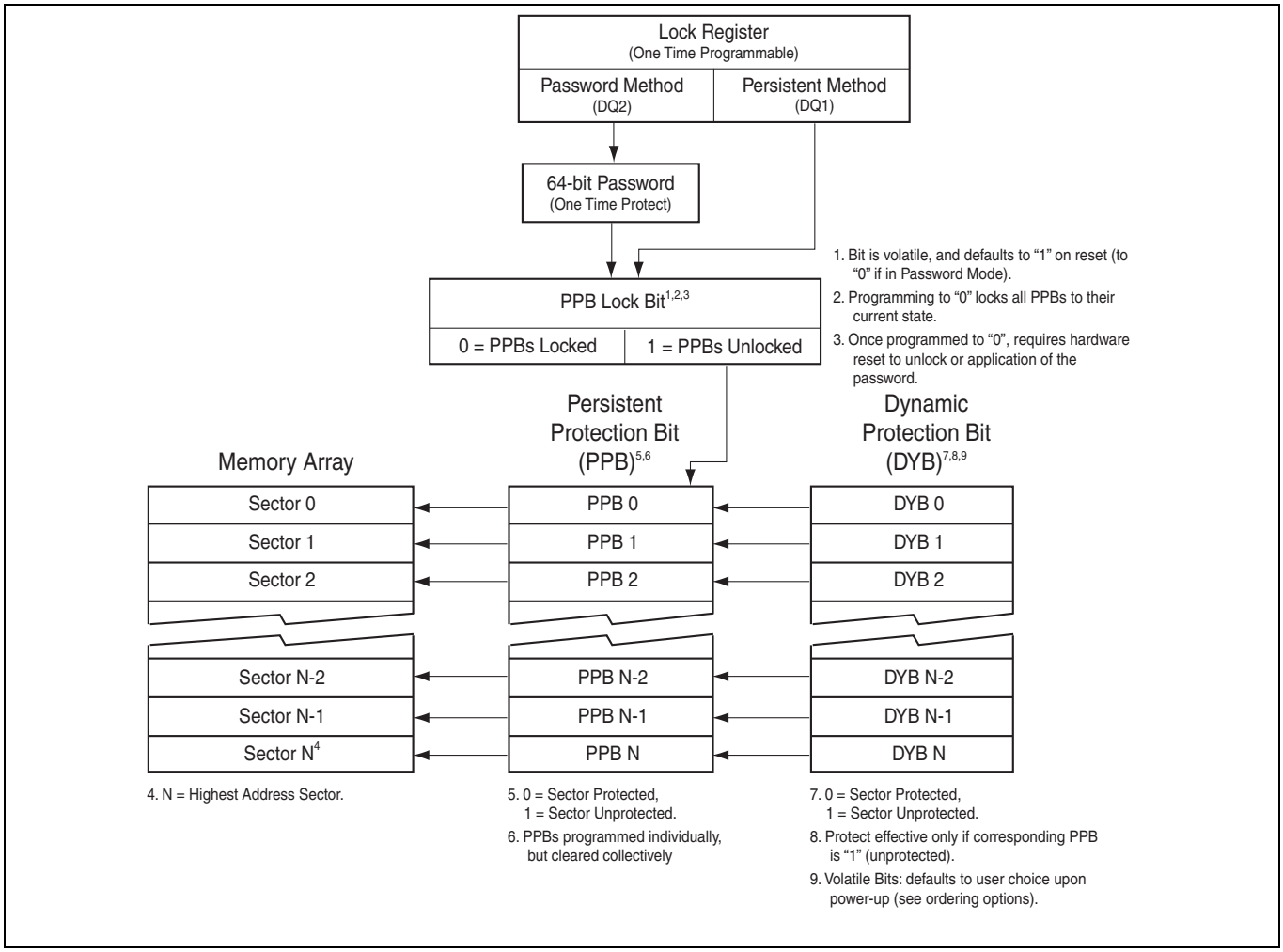


Figure 2 Advanced sector protection overview

Every main flash array sector has a non-volatile (PPB) and a volatile (DYB) protection bit associated with it. When either bit is '0', the sector is protected from program and erase operations.

The PPB bits are protected from program and erase when the PPB Lock bit is '0'. There are two methods for managing the state of the PPB lock bit, persistent protection and password protection.

The persistent protection method sets the PPB lock to ‘1’ during POR or hardware reset so that the PPB bits are unprotected by a device reset. There is a command to clear the PPB lock bit to ‘0’ to protect the PPB bits. There is no command in the persistent protection method to set the PPB lock bit therefore the PPB lock bit will remain at ‘0’ until the next power-off or hardware reset. The persistent protection method allows boot code the option of changing sector protection by programming or erasing the PPB, then protecting the PPB from further change for the remainder of normal system operation by clearing the PPB lock bit. This is sometimes called boot-code controlled sector protection.

The password method clears the PPB lock bit to ‘0’ during POR or hardware reset to protect the PPB. A 64-bit password may be permanently programmed and hidden for the password method. A command can be used to provide a password for comparison with the hidden password. If the password matches the PPB lock bit is set to ‘1’ to unprotect the PPB. A command can be used to clear the PPB lock bit to ‘0’.

The selection of the PPB lock management method is made by programming OTP bits in the lock register so as to permanently select the method used.

The lock register also contains OTP bits, for protecting the SSR.

The PPB bits are erased so that all main flash array sectors are unprotected when shipped from Infineon. The secured silicon region can be factory protected or left unprotected depending on the ordering option (model) ordered.

3.4.3 PPB lock

The persistent protection bit lock is a volatile bit for protecting all PPB bits. When cleared to ‘0’, it locks all PPBs and when set to ‘1’, it allows the PPBs to be changed. There is only one PPB lock bit per device.

The PPB lock command is used to clear the bit to ‘0’. The PPB lock bit must be cleared to ‘0’ only after all the PPBs are configured to the desired settings.

In persistent protection mode, the PPB lock is set to ‘1’ during POR or a hardware reset. When cleared, no software command sequence can set the PPB lock, only another hardware reset or power-up can set the PPB lock bit.

In the password protection mode, the PPB lock is cleared to ‘0’ during POR or a hardware reset. The PPB lock can only set to ‘1’ by the password unlock command sequence. The PPB lock can be cleared by the PPB lock bit clear command.

3.4.4 Persistent protection bits (PPB)

The persistent protection bits (PPB) are located in a separate nonvolatile flash array. One of the PPB bits is assigned to each sector. When a PPB is ‘0’ its related sector is protected from program and erase operations. The PPB are programmed individually but must be erased as a group, similar to the way individual words may be programmed in the main array but an entire sector must be erased at the same time. Preprogramming and verification prior to erasure are handled by the EAC.

Programming a PPB bit requires the typical word programming time. During a PPB bit programming operation or PPB bit erasing, data polling status DQ6 Toggle Bit I will toggle until the operation is complete. Erasing all the PPBs requires typical sector erase time.

If the PPB lock is ‘0’, the PPB program or erase commands do not execute and time-out without programming or erasing the PPB.

The protection state of a PPB for a given sector can be verified by executing a PPB status read command when entered in the PPB ASO.

3.4.5 Dynamic protection bits (DYB)

Dynamic protection bits are volatile and unique for each sector and can be individually modified. DYBs only control protection for sectors that have their PPBs erased. By issuing the DYB set or clear command sequences, the DYB are set to ‘0’ or cleared to ‘1’, thus placing each sector in the protected or unprotected state respectively, if the PPB for the Sector is ‘1’. This feature allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed.

The DYB can be set to ‘0’ or cleared to ‘1’ as often as needed.

3.4.6 Sector protection states summary

Each sector can be in one of the following protection states:

- Unlocked – The sector is unprotected and protection can be changed by a simple command. The protection state defaults to unprotected after a power cycle or hardware reset.
- Dynamically locked – A sector is protected and protection can be changed by a simple command. The protection state is not saved across a power cycle or hardware reset.
- Persistently locked – A sector is protected and protection can only be changed if the PPB lock bit is set to '1'. The protection state is non-volatile and saved across a power cycle or hardware reset. Changing the protection state requires programming or erase of the PPB bits.

Table 11 Sector protection states

Protection bit values			Sector state
PPB lock	PPB	DYB	
1	1	1	Unprotected - PPB and DYB are changeable
1	1	0	Protected - PPB and DYB are changeable
1	0	1	Protected - PPB and DYB are changeable
1	0	0	Protected - PPB and DYB are changeable
0	1	1	Unprotected - PPB not changeable, DYB is changeable
0	1	0	Protected - PPB not changeable, DYB is changeable
0	0	1	Protected - PPB not changeable, DYB is changeable
0	0	0	Protected - PPB not changeable, DYB is changeable

3.4.7 Lock register

The lock register holds the non-volatile OTP bits for controlling protection of the SSR, and determining the PPB lock bit management method (protection mode).

Table 12 Lock register

Bit	Default value	Name
15–9	1	Reserved
8	0	Reserved
7	X	Reserved
6	1	SSR Region 1 (Customer) lock bit
5	1	Reserved
4	1	Reserved
3	1	Reserved
2	1	Password protection mode lock bit
1	1	Persistent protection mode lock bit
0	0	SSR Region 0 (Factory) lock bit

The secure silicon region (SSR) protection bits must be used with caution, as once locked, there is no procedure available for unlocking the protected portion of the secure silicon region and none of the bits in the protected secure silicon region memory space can be modified in any way. Once the secure silicon region area is protected, any further attempts to program in the area will fail with status indicating the area being programmed is protected. The region 0 indicator bit is located in the lock register at bit location 0 and region 1 in bit location 6.

As shipped from the factory, all devices default to the persistent protection method, with all sectors unprotected, when power is applied. The device programmer or host system can then choose which sector protection method to use. Programming either of the following two, one-time programmable, non-volatile bits, locks the part permanently in that mode:

- Persistent protection mode lock bit (DQ1)
- Password protection mode lock bit (DQ2)

If both lock bits are selected to be programmed at the same time, the operation will abort. Once the password mode lock bit is programmed, the persistent mode lock bit is permanently disabled and no changes to the protection scheme are allowed. Similarly, if the persistent mode lock bit is programmed, the password mode is permanently disabled.

If the password mode is to be chosen, the password must be programmed prior to setting the corresponding lock register bit. Setting the password protection mode lock bit is programmed, a power cycle, hardware reset, or PPB lock bit set command is required to set the PPB lock bit to '0' to protect the PPB array.

The programming time of the lock register is the same as the typical word programming time. During a lock register programming EA, data polling status DQ6 Toggle Bit I will toggle until the programming has completed. The system can also determine the status of the lock register programming by reading the status register. See **"Status register"** on page 36 for information on these status bits.

The user is not required to program DQ2 or DQ1, and DQ6 or DQ0 bits at the same time. This allows the user to lock the SSR before or after choosing the device protection scheme. When programming the lock bits, the reserved bits must be '1' (masked).

3.4.8 Persistent protection mode

The persistent protection method sets the PPB lock to '1' during POR or hardware reset so that the PPB bits are unprotected by a device reset. There is a command to clear the PPB lock bit to '0' to protect the PPB. There is no command in the persistent protection method to set the PPB lock bit to '1' therefore the PPB Lock bit will remain at '0' until the next power-off or hardware reset.

3.4.9 Password protection mode

3.4.9.1 PPB password protection mode

PPB password protection mode allows an even higher level of security than the persistent sector protection mode, by requiring a 64-bit password for setting the PPB lock. In addition to this password requirement, after power up and reset, the PPB lock is cleared to '0' to ensure protection at power-up. Successful execution of the password unlock command by entering the entire password sets the PPB lock to '1', allowing for sector PPB modifications.

Password protection notes:

- The password program command is only capable of programming 0's.
- The password is all 1's when shipped from Infineon. It is located in its own memory space and is accessible through the use of the password program and password read commands.
- All 64-bit password combinations are valid as a password.
- Once the password is programmed and verified, the password mode locking bit must be set in order to prevent reading or modification of the password.
- The password mode lock bit, once programmed, prevents reading the 64-bit password on the data bus and further password programming. All further program and read commands to the password region are disabled (data is read as 1's) and these commands are ignored. There is no means to verify what the password is after the password protection mode lock bit is programmed. Password verification is only allowed before selecting the password protection mode.
- The password mode lock bit is not erasable.
- The exact password must be entered in order for the unlocking function to occur.

- The addresses can be loaded in any order but all 4 words are required for a successful match to occur.
- The sector addresses and word line addresses are compared while the password address/data are loaded. If the sector address don't match than the error will be reported at the end of that write cycle. The status register will return to the ready state with the program status bit set to '1', program status register bit set to '1', and write buffer abort status bit set to '1' indicating a failed programming operation. It is a failure to change the state of the PPB lock bit because it is still protected by the lack of a valid password. The data polling status will remain active, with DQ7 set to the complement of the DQ7 bit in the last word of the password unlock command, and DQ6 toggling. RY/BY# will remain LOW.
- The specific address and data are compared after the program buffer to flash command has been given. If they don't match to the internal set value than the status register will return to the ready state with the program status bit set to '1' and program status register bit set to '1' indicating a failed programming operation. It is a failure to change the state of the PPB lock bit because it is still protected by the lack of a valid password. The data polling status will remain active, with DQ7 set to the complement of the DQ7 bit in the last word of the password unlock command, and DQ6 toggling. RY/BY# will remain LOW.
- The device requires approximately 100 µs for setting the PPB Lock after the valid 64-bit password is given to the device.
- The password unlock command cannot be accepted any faster than once every 100 µs ± 20 µs. This makes it take an unreasonably long time (58 million years) for a hacker to run through all the 64-bit combinations in an attempt to correctly match a password. The EA status checking methods may be used to determine when the EAC is ready to accept a new password command.
- If the password is lost after setting the password mode lock bit, there is no way to clear the PPB lock.

4 Read operations

4.1 Asynchronous read

Each read access may be made to any location in the memory (random access). Each random access is self-timed with the same latency from CE# or address to valid data (t_{ACC} or t_{CE}).

4.2 Page mode read

Each random read accesses an entire 32-byte page in parallel. Subsequent reads within the same page have faster read access speed. The page is selected by the higher address bits (A_{MAX}–A4), while the specific word of that page is selected by the least significant address bits A3–A0. The higher address bits are kept constant and only A3–A0 changed to select a different word in the same page. This is an asynchronous access with data appearing on DQ15–DQ0 when CE# remains LOW, OE# remains LOW, and the asynchronous page access time (t_{PACC}) is satisfied. If CE# goes HIGH and returns LOW for a subsequent access, a random read access is performed and time is required (t_{ACC} or t_{CE}).

5 Embedded operations

5.1 Embedded algorithm controller (EAC)

The EAC takes commands from the host system for programming and erasing the flash memory array and performs all the complex operations needed to change the non-volatile memory state. This frees the host system from any need to manage the program and erase processes.

There are four EAC operation categories:

- Standby (Read mode)
- Address space switching
- Embedded algorithms (EA)
- Advanced sector protection (ASP) management

5.1.1 EAC standby

In the standby mode current consumption is greatly reduced. The EAC enters its standby mode when no command is being processed and no embedded algorithm is in progress. If the device is deselected (CE# = HIGH) during an embedded algorithm, the device still draws active current until the operation is completed (I_{CC3}). I_{CC4} in **"DC characteristics"** on page 78 represents the standby current specification when both the Host Interface and EAC are in their standby state.

5.1.2 Address space switching

Writing specific address and data sequences (command sequences) switch the memory device address space from the main flash array to one of the address space overlays (ASO).

Embedded algorithms operate on the information visible in the currently active (entered) ASO. The system continues to have access to the ASO until the system issues an ASO exit command, performs a hardware RESET, or until power is removed from the device. An ASO exit command switches from an ASO back to the main flash array address space. The commands accepted when a particular ASO is entered are listed between the ASO enter and exit commands in the command definitions table. See **"Command summary"** on page 58 for address and data requirements for all command sequences.

5.1.3 Embedded algorithms (EA)

Changing the non-volatile data in the memory array requires a complex sequence of operations that are called embedded algorithms (EA). The algorithms are managed entirely by the device internal embedded algorithm controller (EAC). The main algorithms perform programming and erasing of the main array data and the ASO's. The host system writes command codes to the flash device address space. The EAC receives the commands, performs all the necessary steps to complete the command, and provides status information during the progress of an EA.

5.2 Program and erase summary

Flash data bits are erased in parallel in a large group called a sector. The Erase operation places each data bit in the sector in the logical 1 state (HIGH). Flash data bits may be individually programmed from the erased 1 state to the programmed logical 0 (LOW) state. A data bit of 0 cannot be programmed back to '1'. A succeeding read shows that the data is still '0'. Only erase operations can convert '0' to '1'. Programming the same word location more than once with different 0 bits will result in the logical AND of the previous data and the new data being programmed.

The duration of program and erase operations is shown in **"Embedded Algorithm Performance table"** on page 46.

Program and erase operations may be suspended.

- An erase operation may be suspended to allow either programming or reading of another sector (not in the erase sector). No other erase operation can be started during an erase suspend.
- A program operation may be suspended to allow reading of another location (not in the line being programmed).
- No other program or erase operation may be started during a suspended program operation - program or erase commands will be ignored during a suspended program operation.
- After an intervening program operation or read access is complete the suspended erase or program operation may be resumed. The resume can happen at any time after the suspend assuming the device is not in the process of executing another command.
- Program and erase operations may be interrupted as often as necessary but in order for a program or erase operation to progress to completion there must be some periods of time between resume and the next suspend commands greater than or equal to t_{PRS} or t_{ERS} in **"Embedded Algorithm Performance table"** on page 46.
- When an embedded algorithm (EA) is complete, the EAC returns to the operation state and address space from which the EA was started (Erase suspend or EAC standby).

The system can determine the status of a program or erase operation by reading the status register or using data polling status. Refer to **"Status register"** on page 36 for information on these status bits. Refer to **"Data Polling Status"** on page 38 for more information.

Any commands written to the device during the embedded program algorithm are ignored except the program suspend, and status read command.

Any commands written to the device during the embedded erase algorithm are ignored except erase suspend and status read command.

A hardware reset immediately terminates any in progress program / erase operation and returns to read mode after t_{RPH} time. The terminated operation should be reinitiated once the device has returned to the idle state, to ensure data integrity.

For performance and reliability reasons reading and programming is internally done on full 32-byte pages.

I_{CC3} in **"DC characteristics"** on page 78 represents the active current specification for a write (embedded algorithm) operation.

5.2.1 Program granularity

The S29GL-S supports two methods of programming, word or write buffer programming. Each page can be programmed by either method. Pages programmed by different methods may be mixed within a line for the industrial temperature version (–40°C to +85°C). For the in-cabin version (–40°C to +105°C) the device will only support one programming operation on each 32-byte page between erase operations and single word programming command is not supported.

Word programming examines the data word supplied by the command and programs 0's in the addressed memory array word to match the 0's in the command data word.

Write buffer programming examines the write buffer and programs 0's in the addressed memory array pages to match the 0's in the write buffer. The write buffer does not need to be completely filled with data. It is allowed to program as little as a single bit, several bits, a single word, a few words, a page, multiple Pages, or the entire buffer as one programming operation. Use of the write buffer method reduces host system overhead in writing program commands and reduces memory device internal overhead in programming operations to make write buffer programming more efficient and thus faster than programming individual words with the word programming command.

5.2.2 Incremental programming

The same word location may be programmed more than once, by either the word or write buffer programming methods, to incrementally change 1's to 0's. Note that if additional programming is performed on a page its ECC coverage is disabled.

5.3 Automatic ECC

5.3.1 ECC overview

The automatic ECC feature works transparently with normal program, erase, and read operations. As the device transfers each page of data from the write buffer is to the memory array, internal ECC logic programs ECC code for the page into a portion of the memory array that is not visible to the host system. The device evaluates the page data and the ECC code during each initial page access. If needed, the internal ECC logic corrects a one bit error during the initial access.

Programming more than once to a particular page will disable the ECC function for that page. The ECC function will remain disabled for that page until the next time the host system erases the sector containing that page. The host system may read data stored in that page following multiple programming operations; however, ECC is disabled and an error in that page will not be detected or corrected.

5.3.2 Program and erase summary

For performance and reliability reasons, GL-S devices perform reading and programming on full 32-byte pages in parallel. The GL-S device provides ECC on each page by adding an ECC code to each page when it is first programmed. The ECC code is automatic and transparent to the host system.

5.3.3 ECC implementation

Each 32-byte page in the main flash array and OTP regions features an associated ECC Code. The ECC code, in combination with ECC logic, is able to detect and correct any single bit error found in a page during a read access.

The first write buffer program operation applied to a page programs the ECC code for that page. Subsequent programming operations that occur more than once on a particular page disable the ECC function for that page. This allows bit or word programming; however, note that multiple programming operations to the same page will disable the ECC function on the page where incremental programming occurs. An erase of the sector containing a page with ECC disabled will re-enable the ECC function for that page.

The ECC function is automatic and transparent to the user. The transparency of the automatic ECC function enhances data integrity for typical programming operations that write data once to each page. The ECC function also facilitates software compatibility to previous generations of GL family products by allowing single word programming and bit walking where the same page or word is programmed more than once. When a page has automatic ECC disabled, the ECC function will not detect or correct an error on a data read from that page.

5.3.4 Word programming

Word programming programs a single word anywhere in the main flash memory array. Programming multiple words in the same 32-byte page disables automatic ECC protection on that page. A sector erase of the sector containing that page will re-enable automatic ECC following word programming on that page.

5.3.5 Write buffer programming

Each write buffer program operation allows for programming of 1 bit up to 512 bytes. A 32-byte page is the smallest program granularity that features automatic ECC protection. Programming the same page more than once will disable the automatic ECC on that page. Infineon recommends that a write buffer programming operation program multiple pages in an operation and write each page only once. This keeps the automatic ECC protection enabled on each page. For the very best performance, program in full lines of 512 bytes aligned on 512-byte boundaries.

5.4 Command set

5.4.1 Program methods

5.4.1.1 Word programming

Word programming is used to program a single word anywhere in the main flash memory array.

The word programming command is a four-write-cycle sequence. The program command sequence is initiated by writing two unlock write cycles, followed by the program set up command. The program address and data are written next, which in turn initiate the embedded word program algorithm. The system is not required to provide further controls or timing. The device automatically generates the program pulses and verifies the programmed cell margin internally. When the embedded word program algorithm is complete, the EAC then returns to its standby mode.

The system can determine the status of the program operation by using data polling status, reading the status register, or monitoring the RY/BY# output. See **"Status register"** on page 36 for information on these status bits. See **"Data Polling Status"** on page 38 for information on these status bits. See **Figure 3** for a diagram of the programming operation.

Any commands other than program suspend written to the device during the embedded program algorithm are ignored. Note that a hardware reset (RESET# = V_{IL}) immediately terminates the programming operation and returns the device to read mode after t_{RPH} time. To ensure data integrity, the program command sequence should be reinitiated once the device has completed the hardware reset operation.

A modified version of the word programming command, without unlock write cycles, is used for programming when entered into the lock register, password, and PPB ASOs. The same command is used to change volatile bits when entered in to the PPB Lock, and DYB ASOs. See **Table 41** for program command sequences.

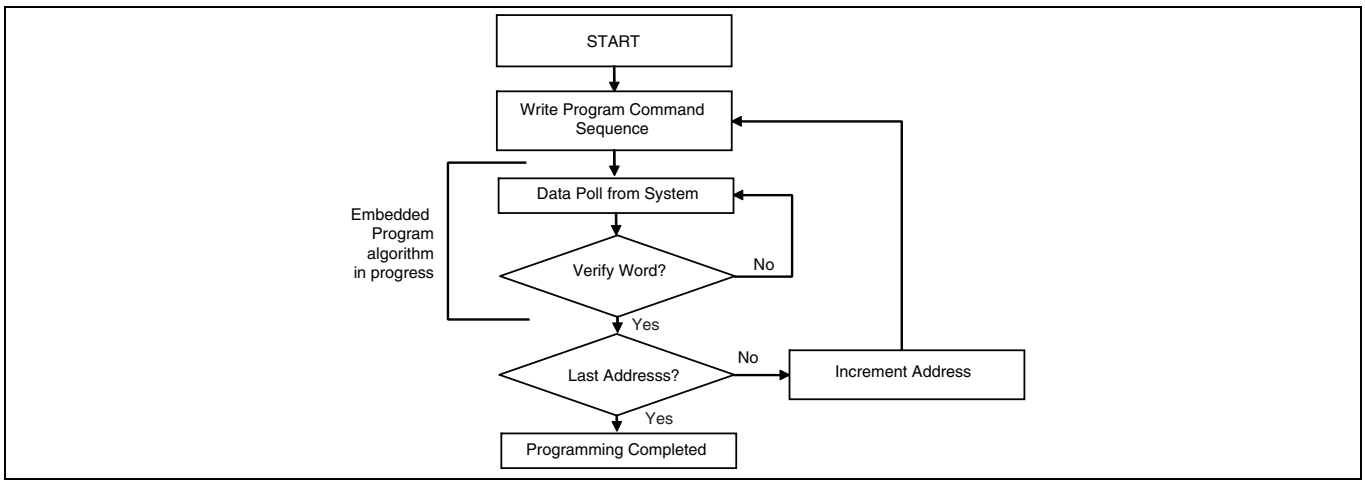


Figure 3 Word program operation

5.4.1.2 Write buffer programming

A write buffer is used to program data within a 512-byte address range aligned on a 512-byte boundary (Line). Thus, a full write buffer programming operation must be aligned on a line boundary. Programming operations of less than a full 512 bytes may start on any word boundary but may not cross a Line boundary. At the start of a write buffer programming operation all bit locations in the buffer are all 1's (FFFFh words) thus any locations not loaded will retain the existing data. See **"Product overview"** on page 5 for information on address map.

Write buffer programming allows up to 512 bytes to be programmed in one operation. It is possible to program from 1 bit up to 512 bytes in each write buffer programming operation. It is recommended that a multiple of pages be written and each page written only once. For the very best performance, programming should be done in full lines of 512 bytes aligned on 512-byte boundaries.

Write buffer programming is supported only in the main flash array or the SSR ASO.

The write buffer programming operation is initiated by first writing two unlock cycles. This is followed by a third write cycle of the write to buffer command with the sector address (SA), in which programming is to occur. Next, the system writes the number of word locations minus 1. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the program buffer to flash confirm command. The sector address must match in the write to buffer command and the write word count command. The sector to be programmed must be unlocked (unprotected).

The system then writes the starting address / data combination. This starting address is the first address / data pair to be programmed, and selects the write-buffer-line address. The sector address must match the write to buffer sector address or the operation will abort and return to the initiating state. All subsequent address / data pairs must be in sequential order. All write buffer addresses must be within the same line. If the system attempts to load data outside this range, the operation will abort and return to the initiating state.

The counter decrements for each data load operation. Note that while counting down the data writes, every write is considered to be data being loaded into the write buffer. No commands are possible during the write buffer loading period. The only way to stop loading the write buffer is to write with an address that is outside the line of the programming operation. This invalid address will immediately abort the write to buffer command.

Once the specified number of write buffer locations has been loaded, the system must then write the program buffer to flash command at the sector address. The device then goes busy. The embedded program algorithm automatically programs and verifies the data for the correct data pattern. The system is not required to provide any controls or timings during these operations. If an incorrect number of write buffer locations have been loaded the operation will abort and return to the initiating state. The abort occurs when anything other than the program buffer to flash is written when that command is expected at the end of the word count.

The write-buffer embedded programming operation can be suspended using the program suspend command. When the embedded program algorithm is complete, the EAC then returns to the EAC standby or erase suspend standby state where the programming operation was started.

The system can determine the status of the program operation by using data polling status, reading the status register, or monitoring the RY/BY# output. See **"Status register"** on page 36 for information on these status bits. See **"Data Polling Status"** on page 38 for information on these status bits. See **Figure 4** for a diagram of the programming operation.

The write buffer programming sequence will be aborted under the following conditions:

- Load a word count value greater than the buffer size (255).
- Write an address that is outside the line provided in the write to buffer command.
- The program buffer to flash command is not issued after the write word count number of data words is loaded.

When any of the conditions that cause an abort of write buffer command occur the abort will happen immediately after the offending condition, and will indicate a program fail in the status register at bit location 4 (PSB = 1) due to write buffer abort bit location 3 (WBASB = 1). The next successful program operation will clear the failure status or a clear status register may be issued to clear the PSB status bit.

The write buffer programming sequence can be stopped by the following: Hardware reset or power cycle. However, these using either of these methods may leave the area being programmed in an intermediate state with invalid or unstable data values. In this case the same area will need to be reprogrammed with the same data or erased to ensure data values are properly programmed or erased.

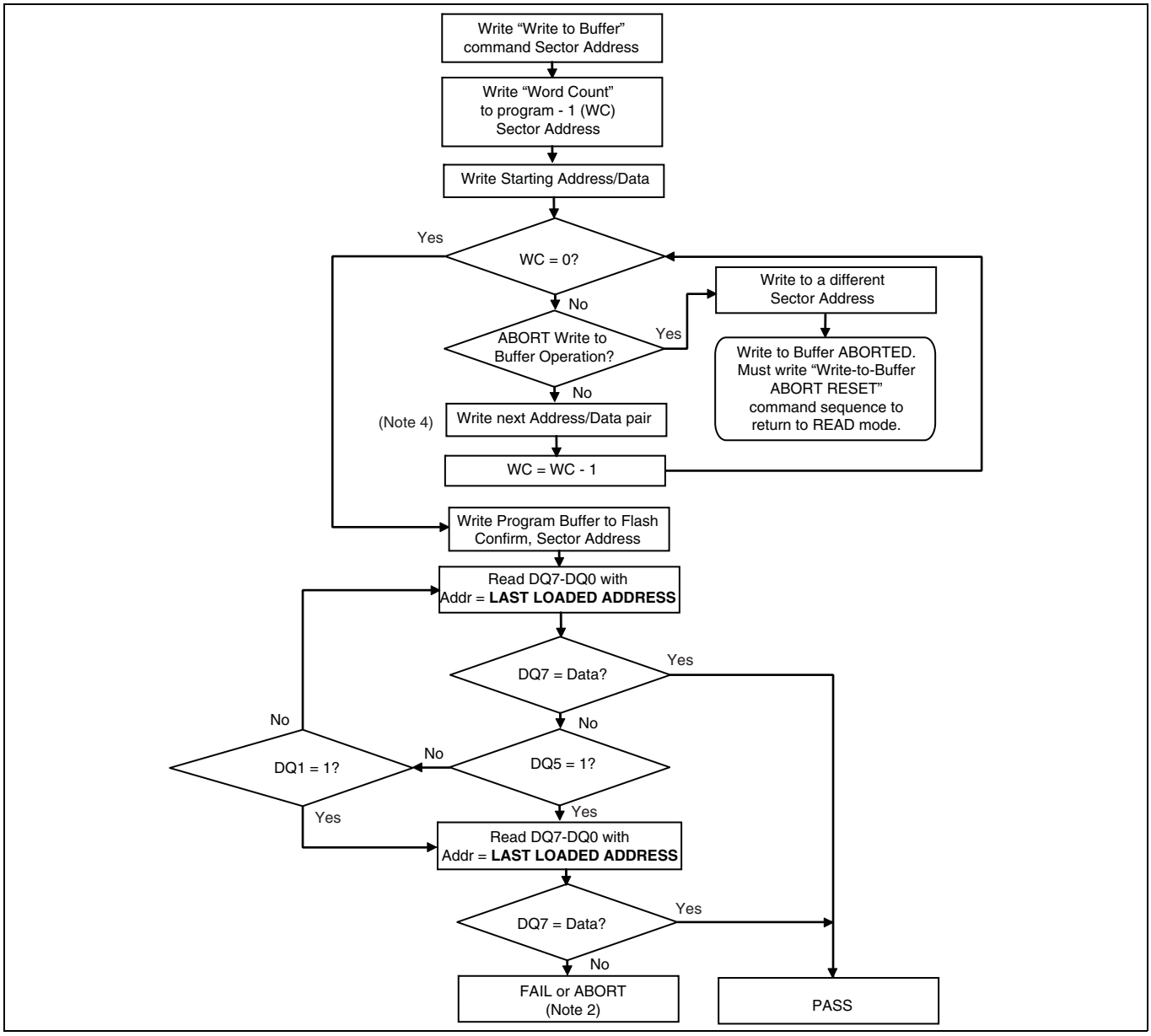


Figure 4 Write buffer programming operation with data polling status

Notes

1. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.
2. If this flowchart location was reached because DQ5 = 1, then the device FAILED. If this flowchart location was reached because DQ1 = 1, then the Write Buffer operation was ABORTED. In either case the proper RESET command must be written to the device to return the device to READ mode.
   Write-Buffer-Programming-Abort-Rest if DQ1 = 1, either Software RESET or
   Write-Buffer-Programming-Abort-Reset if DQ5 = 1.
3. See **Table 41** for the command sequence as required for write buffer programming.
4. When sector address is specified, any address in the selected sector is acceptable. However, when loading write-buffer address locations with data, all addresses must fall within the selected write-buffer page.

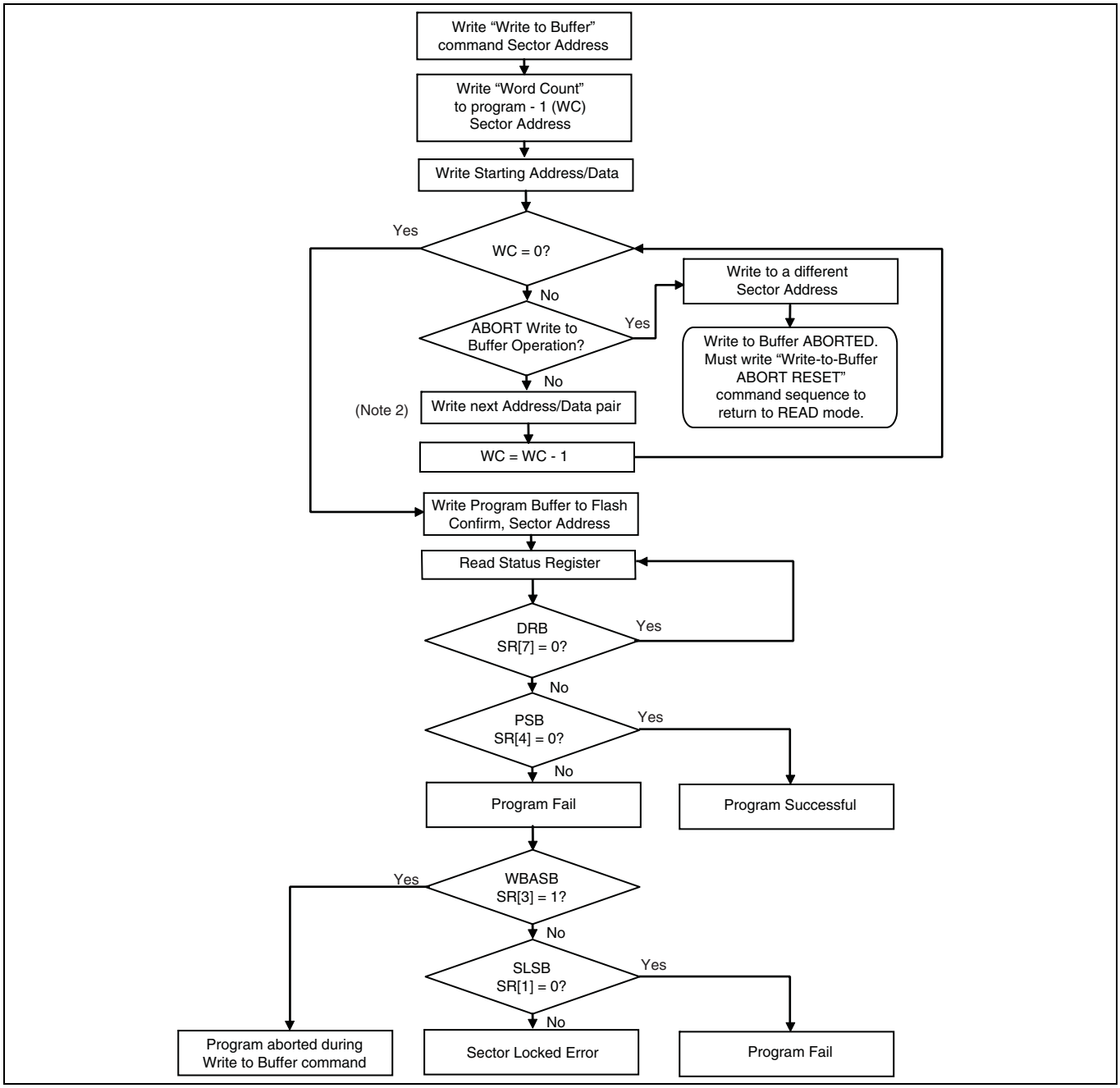


Figure 5 Write buffer programming operation with status register

Notes

5. See **Table 41** for the command sequence as required for write buffer programming.
6. When sector address is specified, any address in the selected sector is acceptable. However, when loading write-buffer address locations with data, all addresses must fall within the selected write-buffer page.

Table 13 Write buffer programming command sequence

Sequence	Address	Data	Comment
Issue Unlock Command 1	555/AAA	AA	
Issue Unlock Command 2	2AA/555	55	
Issue Write to Buffer Command at sector address	SA	0025h	
Issue number of locations at sector address	SA	WC	WC = number of words to program – 1
Example: WC of 0 = 1 words to pgm			
WC of 1 = 2 words to pgm			
Load starting Address / Data pair	Starting address	PD	Selects Write-Buffer-Page and loads first Address/Data pair.
Load next Address / Data pair	WBL	PD	All addresses must be within the selected write-buffer-page boundaries, and have to be loaded in sequential order.
Load last Address/Data pair	WBL	PD	All addresses must be within the selected write-buffer-page boundaries, and have to be loaded in sequential order.
Issue Write Buffer Program Confirm at sector address	SA	0029h	This command must follow the last write buffer location loaded, or the operation will abort.
Device goes busy.			

Legend:
SA = Sector address (Non-sector address bits are don't care. Any address within the sector is sufficient.)
WBL = Write buffer location (Must be within the boundaries of the Write-Buffer-Line specified by the starting address.)
WC = Word count
PD = Program data

5.4.2 Program Suspend / Program Resume commands

The Program Suspend command allows the system to interrupt an embedded programming operation so that data can read from any non-suspended line. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are don't-cares when writing the Program Suspend command.

There are two commands available for program suspend. The legacy combined Erase / Program suspend command (B0h command code) and the separate Program Suspend command (51h command code). There are also two commands for Program resume. The legacy combined Erase / Program resume command (30h command code) and the separate Program Resume command (50h command code). It is recommended to use the separate program suspend and resume commands for programming and use the legacy combined command only for erase suspend and resume.

After the programming operation has been suspended, the system can read array data from any non-suspended Line. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend.

After the Program Resume command is written, the device reverts to programming and the status bits are updated. The system can determine the status of the program operation by reading the status register or using data polling. Refer to **"Status register"** on page 36 for information on these status bits. Refer to **"Data Polling Status"** on page 38 for more information.

Accesses and commands that are valid during Program Suspend are:

- Read to any other non-erase-suspended sector
- Read to any other non-program-suspended line
- Status Read command
- Exit ASO or Command Set Exit
- Program Resume command

The system must write the Program Resume command to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Program operations can be interrupted as often as necessary but in order for a program operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{PRS} in **"Embedded algorithm controller (EAC)"** on page 21.

Program suspend and resume is not supported while entered in an ASO. While in program suspend entry into ASO is not supported.

5.4.3 Blank Check

The Blank Check command will confirm if the selected main flash array sector is erased. The Blank Check command does not allow for reads to the array during the Blank Check. Reads to the array while this command is executing will return unknown data.

To initiate a Blank Check on a sector, write 33h to address 555h in the sector, while the EAC is in the standby state

The Blank Check command may not be written while the device is actively programming or erasing or suspended.

Use the status register read to confirm if the device is still busy and when complete if the sector is blank or not. Bit 7 of the status register will show if the device is performing a Blank Check (similar to an erase operation). Bit 5 of the status register will be cleared to '0' if the sector is erased and set to '1' if not erased.

As soon as any bit is found to not be erased, the device will halt the operation and report the results.

Once the Blank Check is completed, the EAC will return to the Standby State.

5.4.4 Erase methods

5.4.4.1 Chip Erase

The chip erase function erases the entire main flash memory array. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all 0 data pattern prior to electrical erase. After a successful chip erase, all locations within the device contain FFFFh. The system is not required to provide any controls or timings during these operations. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. When WE# goes HIGH, at the end of the 6th cycle, the RY/BY# goes LOW.

When the embedded erase algorithm is complete, the EAC returns to the standby state. Note that while the embedded erase operation is in progress, the system can not read data from the device. The system can determine the status of the erase operation by reading RY/BY#, the status register or using data polling. Refer to **"Status register"** on page 36 for information on these status bits. Refer to **"Data Polling Status"** on page 38 for more information.

Once the chip erase operation has begun, only a status read, hardware reset or power cycle are valid. All other commands are ignored. However, a hardware reset or power cycle immediately terminates the erase operation and returns to read mode after t_{RPH} time. If a chip erase operation is terminated, the chip erase command sequence must be reinitiated once the device has returned to the idle state to ensure data integrity.

See **Table 16**, **"Asynchronous Write Operations"** on page 90 and **"Alternate CE# Controlled Write operations"** on page 98 for parameters and timing diagrams.

Sectors protected by the ASP DYB and PPB lock bits will not be erased. See **"ASP"** on page 15. If a sector is protected during chip erase, chip erase will skip the protected sector and continue with next sector erase. The status register erase status bit and sector lock bit are not set to '1' by a failed erase on a protected sector.

5.4.4.2 Sector Erase

The sector erase function erases one sector in the memory array. The device does not require the system to preprogram prior to erase. The embedded erase algorithm automatically programs and verifies the entire sector for an all 0 data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. When WE# goes HIGH, at the end of the 6th cycle, the RY/BY# goes LOW.

The system can determine the status of the erase operation by reading the status register or using data polling. Refer to **"Status register"** on page 36 for information on these status bits. Refer to **"Data Polling Status"** on page 38 for more information.

Once the sector erase operation has begun, the Status Register Read and Erase Suspend commands are valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation and returns to read mode after t_{RPH} time. If a sector erase operation is terminated, the sector erase command sequence must be reinitiated once the device has reset operation to ensure data integrity.

See **"Embedded algorithm controller (EAC)"** on page 21 for parameters and timing diagrams.

Sectors protected by the ASP DYB and PPB lock bits will not be erased. See **"ASP"** on page 15.

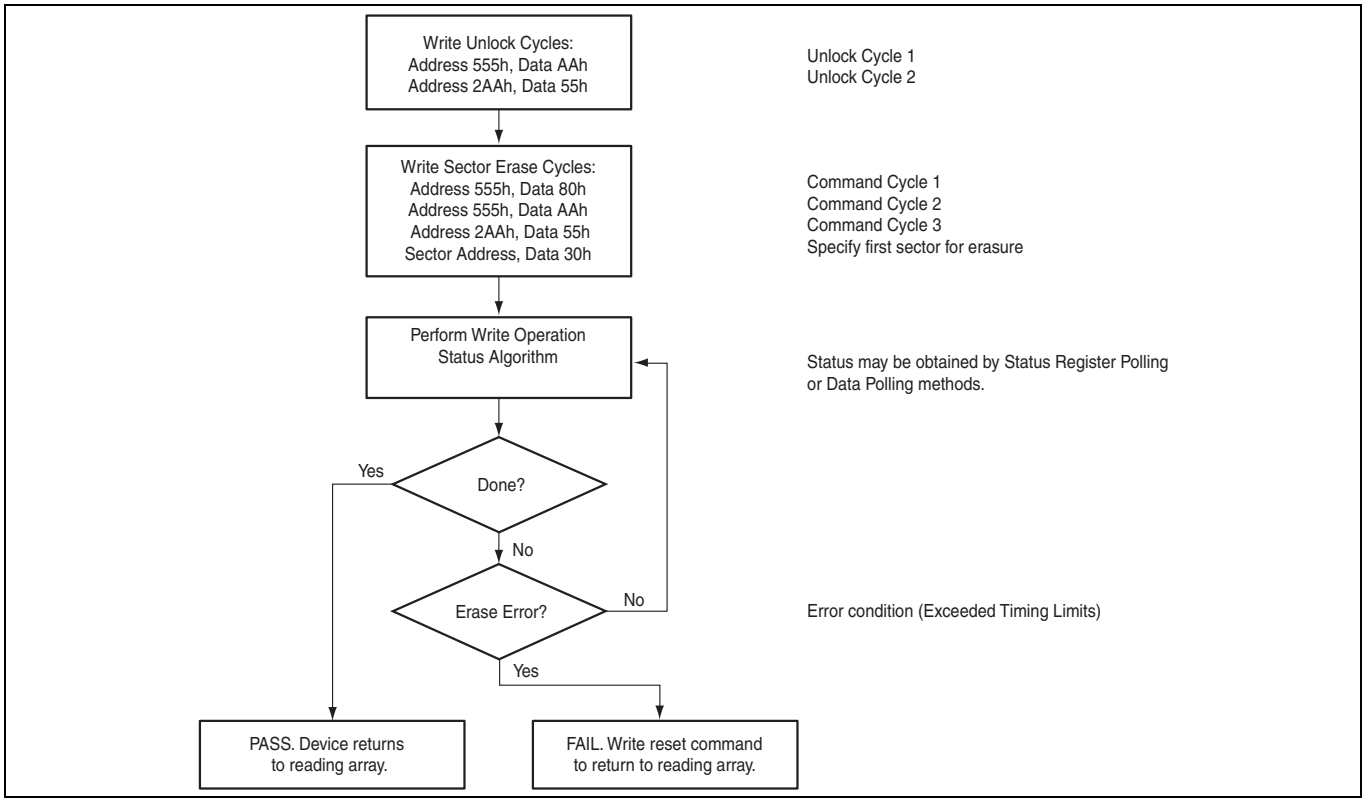


Figure 6 Sector Erase operation

5.4.5 Erase Suspend / Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, the main flash array. This command is valid only during sector erase or program operation. The Erase Suspend command is ignored if written during the chip erase operation.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of t_{ESL} (erase suspend latency) to suspend the erase operation and update the status bits.

After the erase operation has been suspended, the part enters the erase-suspend mode. The system can read data from or program data to the main flash array. Reading at any address within erase-suspended sectors produces undetermined data. The system can determine if a sector is actively erasing or is erase-suspended by reading the status register or using data polling. Refer to **"Status register"** on page 36 for information on these status bits. Refer to **"Data Polling Status"** on page 38 for more information.

After an erase-suspended program operation is complete, the EAC returns to the erase-suspend state. The system can determine the status of the program operation by reading the status register, just as in the standard program operation.

If a program failure occurs during erase suspend the Clear or Reset commands will return the device to the erase suspended state. Erase will need to be resumed and completed before again trying to program the memory array.

Accesses and commands that are valid during Erase Suspend are:

- Read to any other non-suspended sector
- Program to any other non-suspended sector
- Status Register Read
- Status Register Clear
- Enter DYB ASO
- DYB Set
- DYB Clear
- DYB Status Read
- Exit ASO or Command Set Exit
- Erase Resume command

To resume the sector erase operation, the system must write the Erase Resume command. The device will revert to erasing and the status bits will be updated. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Erase suspend and resume is not supported while entered in an ASO. While in erase suspend entry into ASO is not supported.

5.4.6 ASO Entry and Exit

5.4.6.1 ID-CFI ASO

The system can access the ID-CFI ASO by issuing the ID-CFI Entry command sequence during Read Mode. This entry command uses the Sector Address (SA) in the command to determine which sector will be overlaid and which sector's protection state is reported in word location 2h. See the detail description **Table 42**.

The ID-CFI ASO allows the following activities:

- Read ID-CFI ASO, using the same SA as used in the entry command.
- Read Sector Protection State at Sector Address (SA) + 2h. Location 2h provides volatile information on the current state of sector protection for the sector addressed. Bit 0 of the word at location 2h shows the logical NAND of the PPB and DYB bits related to the addressed sector such that if the sector is protected by either the PPB = 0 or the DYB = 0 bit for that sector the state shown is protected. (1 = Sector protected, 0 = Sector unprotected). This protection state is shown only for the SA selected when entering ID-CFI ASO. Reading other SA provides undefined data. To read a different SA protection state ASO exit command must be used and then enter ID-CFI ASO again with the new SA.
- ASO Exit.

The following is a C source code example of using the CFI Entry and Exit functions.

```
/* Example: CFI Entry command */
*( (UINT16 *)base_addr + 0x55 ) = 0x0098; /* write CFI entry command */

/* Example: CFI Exit command */
*( (UINT16 *)base_addr + 0x000 ) = 0x00F0; /* write cfi exit command */
```

5.4.6.2 Status Register ASO

The Status Register ASO contains a single word of registered volatile status for embedded algorithms. When the Status Register Read command is issued, the current status is captured (by the rising edge of WE#) into the register and the ASO is entered. The Status Register content appears on all word locations. The first read access exits the Status Register ASO (with the rising edge of CE# or OE#) and returns to the address space map in use when the Status Register Read command was issued. Write commands will not exit the Status Register ASO state.

5.4.6.3 Secure Silicon Region ASO

The system can access the Secure Silicon Region by issuing the Secure Silicon Region Entry command sequence during Read Mode. This entry command uses the Sector Address (SA) in the command to determine which sector will be overlaid.

The Secure Silicon Region ASO allows the following activities:

- Read Secure Silicon Regions.
- Programming the customer Secure Silicon Region is allowed using the Word or Write Buffer Programming commands.
- ASO Exit using legacy Secure Silicon Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.4.6.4 Lock Register ASO

The system can access the lock register by issuing the Lock Register Entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The lock register appears at word location 0 in the device address space. All other locations in the device address space are undefined.

The Lock Register ASO allows the following activities:

- Read Lock Register, using device address location 0.
- Program the customer Lock Register using a modified Word Programming command.
- ASO Exit using legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.4.6.5 Password ASO

The system can access the Password ASO by issuing the Password Entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The password appears at word locations 0 to 3 in the device address space. All other locations in the device address space are undefined.

The Password ASO allows the following activities:

- Read Password, using device address location 0 to 3.
- Program the password using a modified Word Programming command.
- Unlock the PPB lock bit with the Password Unlock command.
- ASO Exit using Legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the Common Exit command for all ASO - alternative for a consistent exit method.

5.4.6.6 PPB ASO

The system can access the PPB ASO by issuing the PPB Entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The PPB bit for a sector appears in bit 0 of all word locations in the sector.

The PPB ASO allows the following activities:

- Read PPB protection status of a sector in bit 0 of any word in the sector.
- Program the PPB bit using a modified Word Programming command.
- Erase all PPB bits with the PPB Erase command.
- ASO Exit using Legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.4.6.7 PPB Lock ASO

The system can access the PPB Lock ASO by issuing the PPB Lock Entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The global PPB Lock bit appears in bit 0 of all word locations in the device.

The PPB Lock ASO allows the following activities:

- Read PPB Lock protection status in bit 0 of any word in the device address space.
- Set the PPB Lock bit using a modified Word Programming command.
- ASO Exit using Legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the Common Exit command for all ASO - alternative for a consistent exit method.

5.4.6.8 DYB ASO

The system can access the DYB ASO by issuing the DYB Entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The DYB bit for a sector appears in bit 0 of all word locations in the sector.

The DYB ASO allows the following activities:

- Read DYB protection status of a sector in bit 0 of any word in the sector.
- Set the DYB bit using a modified Word Programming command.
- Clear the DYB bit using a modified Word Programming command.
- ASO Exit using Legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the Common Exit command for all ASO - alternative for a consistent exit method.

5.4.6.9 Software (Command) Reset / ASO exit

Software reset is part of the command set (see **Table 41**) that also returns the EAC to standby state and must be used for the following conditions:

- Exit ID/CFI mode
- Clear timeout bit (DQ5) for data polling when timeout occurs

Software Reset does not affect EA mode. Reset commands are ignored once programming or erasure has begun, until the operation is complete. Software Reset does not affect outputs; it serves primarily to return to Read Mode from an ASO mode or from a failed program or erase operation.

Software Reset may cause a return to Read Mode from undefined states that might result from invalid command sequences. However, a Hardware Reset may be required to return to normal operation from some undefined states.

There is no software reset latency requirement. The reset command is executed during the t_{WPH} period.

5.4.6.10 ECC Status ASO

The system can access the ECC Status ASO by issuing the ECC Status entry command sequence during Read Mode. The contents of the ECC Status ASO indicates, for the selected ECC page, whether ECC protection has corrected an error in the eight-bit error correction code or the 16 Words of data in the ECC page.

The ECC Status ASO allows the following activities:

- Read ECC Status for the selected page.

5.5 Status monitoring

There are three methods for monitoring EA status. Previous generations of the S29GL flash family used the methods called Data Polling and Ready/Busy# (RY/BY#) signal. These methods are still supported by the S29GL-S family. One additional method is reading the status register.

5.5.1 Status register

The status of program and erase operations is provided by a single 16-bit status register. The status is receiver by writing the Status Register Read command followed by a read access. When the Status Register Read command is issued, the current status is captured (by the rising edge of WE#) into the register and the ASO is entered. The contents of the status register is aliased (overlaid) on the full memory address space. Any valid read (CE# and OE# low) access while in the Status Register ASO will exit the ASO (with the rising edge of CE# or OE# for t_{CEPH}/t_{OEPH} time) and return to the address space map in use when the Status Register Read command was issued.

The status register contains bits related to the results - success or failure - of the most recently completed embedded algorithms (EA):

- Erase Status (bit 5),
- Program Status (bit 4),
- Write Buffer Abort (bit 3),
- Sector Locked Status (bit 1),
- RFU (bit 0).

and, bits related to the current state of any in process EA:

- Device Busy (bit 7),
- Erase Suspended (bit 6),
- Program Suspended (bit 2),

The current state bits indicate whether an EA is in process, suspended, or completed.

The upper 8 bits (bits 15:8) are reserved. These have undefined HIGH or LOW value that can change from one status read to another. These bits should be treated as don’t care and ignored by any software reading status.

The Soft Reset command will clear to 0 bits [5, 4, 1, 0] of the status register if Status Register bit 3 = 0. It will not affect the current state bits. The Clear Status Register Command will clear to 0 the results related bits of the status register but will not affect the current state bits.

Table 14 Status Register

Bit #	15:8	7	6	5	4	3	2	1	0
Bit description	Reserved	Device Ready Bit	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	Write Buffer Abort Status Bit	Program Suspend Status Bit	Sector Lock Status Bit	Reserved
Bit name		DRB	ESSB	ESB	PSB	WBASB	PSSB	SLSB	
Reset status	X	1	0	0	0	0	0	0	0
Busy status	Invalid	0	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Ready status	X	1	0 = No Erase in Suspension 1 = Erase in Suspension	0 = Erase successful 1 = Erase fail	0 = Program successful 1 = Program fail	0 = Program not aborted 1 = Program aborted during Write to Buffer command	0 = No Program in suspension 1 = Program in suspension	0 = Sector not locked during operation 1 = Sector locked error	X

Notes
7. Bits 15 thru 8, and 0 are reserved for future use and may display as ‘0’ or ‘1’. These bits should be ignored (masked) when checking status.
8. Bit 7 is 1 when there is no Embedded Algorithm in progress in the device.
9. Bits 6 thru 1 are valid only if Bit 7 is ‘1’.
10. All bits are put in their reset status by cold reset or warm reset.
11. Bits 5, 4, 3, and 1 are cleared to ‘0’ by the Clear Status Register command or Reset command.
12. Upon issuing the Erase Suspend Command, the user must continue to read status until DRB becomes ‘1’.
13. ESSB is cleared to ‘0’ by the Erase Resume command.
14. ESB reflects success or failure of the most recent erase operation.
15. PSB reflects success or failure of the most recent program operation.
16. During erase suspend, programming to the suspended sector, will cause program failure and set the Program status bit to ‘1’.
17. Upon issuing the Program Suspend command, the user must continue to read status until DRB becomes ‘1’.
18. PSSB is cleared to ‘0’ by the Program Resume command.
19. SLSB indicates that a program or erase operation failed because the sector was locked.
20. SLSB reflects the status of the most recent program or erase operation.

5.5.2 Data Polling Status

During an active embedded algorithm the EAC switches to the Data Polling ASO to display EA status to any read access. A single word of status information is aliased in all locations of the device address space. In the status word there are several bits to determine the status of an EA. These are referred to as DQ bits as they appear on the data bus during a read access while an EA is in progress. DQ bits 15 to 8, DQ4, and DQ0 are reserved and provide undefined data. Status monitoring software must mask the reserved bits and treat them as don't care. **Table 15** and the following subsections describe the functions of the remaining bits.

5.5.2.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an embedded algorithm is in progress or has completed. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence. Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page will return false status information.

During the embedded program algorithm, the device outputs on DQ7 the complement of the data bit programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the embedded program algorithm is complete, the device outputs the data bit programmed to bit 7 of the last word programmed. In case of a Program Suspend, the device allows only reading array data. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 20 µs, then the device returns to reading array data.

During the embedded erase or blank check algorithms, Data# Polling produces a ‘0’ on DQ7. When the algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a ‘1’ on DQ7. This is analogous to the complement / true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to ‘1’; prior to this, the device outputs the complement or ‘0’. The system must provide an address within the sector selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if the sector selected for erasing is protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted Low. This is illustrated in **Figure 29**. **Table 15** shows the outputs for Data# polling on DQ7. **Figure 4** shows the Data# polling algorithm use in Write Buffer Programming.

Valid DQ7 data polling status may only be read from:

- the address of the last word loaded into the write buffer for a write buffer programming operation;
- the location of a single word programming operation;
- or a location in a sector being erased or blank checked;
- or a location in any sector during chip erase.

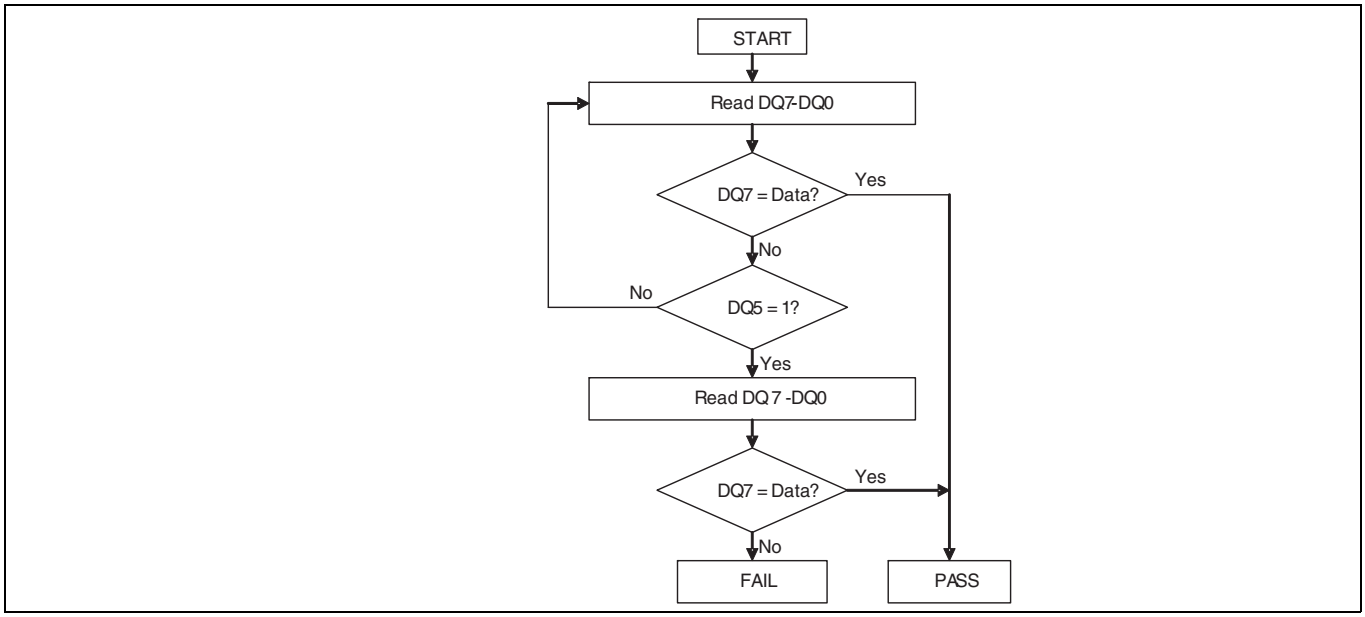


Figure 7 Data# Polling algorithm

5.5.2.2 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an embedded program or erase algorithm is in progress or complete, or whether the device has entered the Program Suspend or Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation).

During an embedded program or erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if the sector selected for erasing is protected, DQ6 toggles for approximately 100 µs, then the EAC returns to standby (Read Mode). If the selected sector is not protected, the embedded erase algorithm erases the unprotected sector.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or erase-suspended. When the device is actively erasing (that is, the embedded erase algorithm is in progress), DQ6 toggles. When the device enters the Program Suspend mode or Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing, or erase-suspended. Alternatively, the system can use DQ7 (see **"DQ7: Data# Polling"** on page 38).

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the embedded program algorithm is complete.

Table 15 shows the outputs for Toggle Bit I on DQ6. **Figure 8** shows the toggle bit algorithm in flowchart form, and the **"Reading Toggle Bits DQ6/DQ2"** on page 40 explains the algorithm. **Figure 8** shows the toggle bit timing diagrams. **Figure 4** shows the differences between DQ2 and DQ6 in graphical form. See also **"DQ2: Toggle Bit II"** on page 40.

Note
21.DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

5.5.2.3 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. See **"Sector Erase"** on page 30 for more details.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is '1', the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. **Table 15** shows the status of DQ3 relative to the other status bits.

5.5.2.4 DQ2: Toggle Bit II

Toggle Bit II on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within the sector selected for erasure. (The system may use either OE# or CE# to control the read cycles). But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish if the sector is selected for erasure. Thus, both status bits are required for sector and mode information. Refer to **Table 15** to compare outputs for DQ2 and DQ6. **Figure 7** shows the toggle bit algorithm in flowchart form, and the **"Reading Toggle Bits DQ6/DQ2"** on page 40 explains the algorithm. See also **Figure 8** shows the toggle bit timing diagram. **Figure 4** shows the differences between DQ2 and DQ6 in graphical form.

5.5.2.5 Reading Toggle Bits DQ6/DQ2

Refer to **Figure 7** for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the previous value. If the toggle bit is not toggling, the device has completed the program or erases operation. The system can read array data on DQ15–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is HIGH (see **"DQ5: Exceeded Timing Limits"** on page 41). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went HIGH. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone HIGH. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of **Figure 8**).

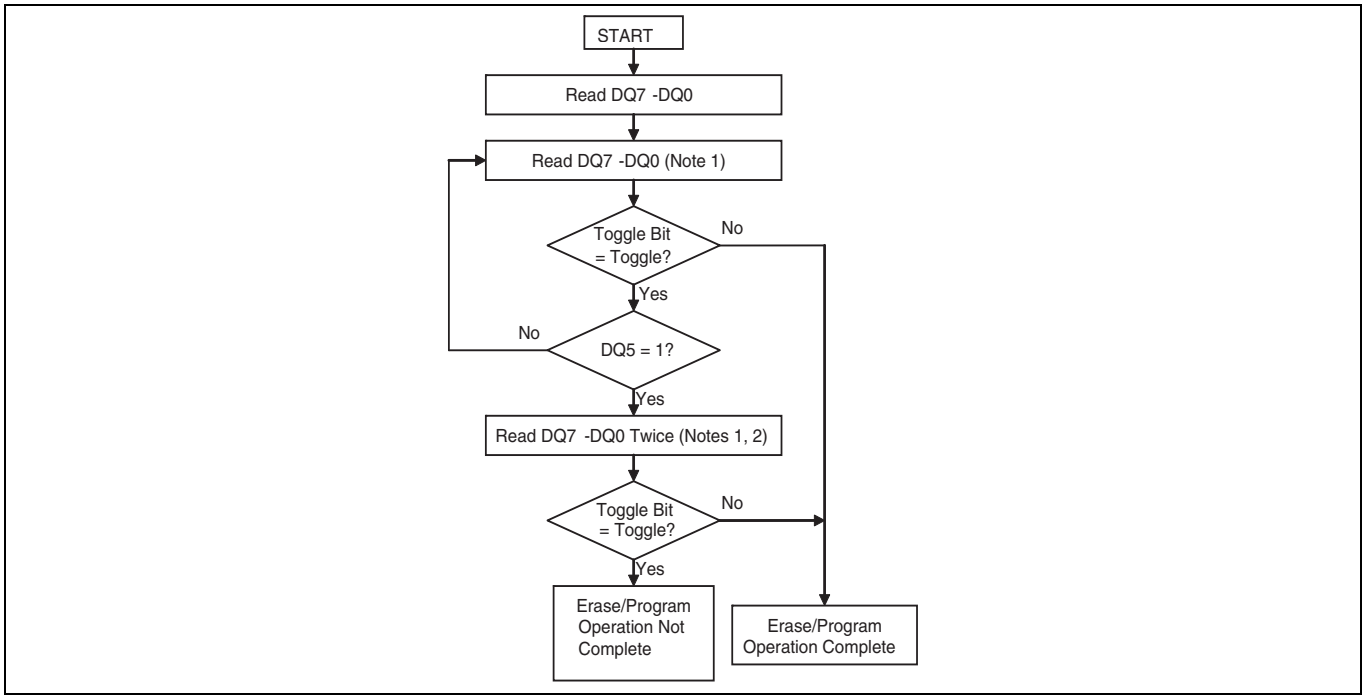


Figure 8 Toggle bit program

5.5.2.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a '1'. This is a failure condition that indicates the program or erase cycle was not successfully completed. The system must issue the reset command to return the device to reading array data.

When a timeout occurs, the software must send a reset command to clear the timeout bit (DQ5) and to return the EAC to read array mode. In this case, it is possible that the flash will continue to communicate busy for up to 2 µs after the reset command is sent.

Notes
22.Read toggle bit twice to determine whether or not it is toggling. See text.
23.Recheck toggle bit because it may stop toggling as DQ5 changes to '1'. See text.

5.5.2.7 DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a '1'. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the EAC to standby (Read Mode) and the status register failed bits are cleared. See **"Write buffer programming"** on page 25 for more details.

Table 15 Data Polling status

Operation		DQ7[24]	DQ6	DQ5[25]	DQ3	DQ2[24]	DQ1[26]	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No Toggle	0	0
	Reading within Erasing Sector	0	Toggle	0	1	Toggle	N/A	0
	Reading Outside erasing Sector	0	Toggle	0	1	No Toggle	N/A	0
Program Suspend Mode[27]	Reading within Program Suspended Sector	INVALID (Not allowed)	INVALID (Not allowed)	INVALID (Not allowed)	INVALID (Not allowed)	INVALID (Not allowed)	INVALID (Not allowed)	1
	Reading within Non-Program Suspended Sector	Data	Data	Data	Data	Data	Data	1
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	N/A	1
	Reading within Non-Erase Suspend Sector	Data	Data	Data	Data	Data	Data	1
	Programming within Non-Erase Suspended Sector	DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer[26, 28]	BUSY State	DQ7#	Toggle	0	N/A	No Toggle	0	0
	Exceeded Timing Limits	DQ7#	Toggle	1	N/A	N/A	0	0
	ABORT State	DQ7#	Toggle	0	N/A	N/A	1	0

Notes

24. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
25. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See **"DQ5: Exceeded Timing Limits"** on page 41 for more information.
26. DQ1 indicates the Write-to-Buffer abort status during Write-Buffer-Programming operations.
27. Data are invalid for addresses in a Program Suspended Line. All addresses other than the program suspended line can be read for valid data.
28. Applies only to program operations.

5.6 Error types and clearing procedures

There are three types of errors reported by the embedded operation status methods. Depending on the error type, the status reported and procedure for clearing the error status is different. Following is the clearing of error status:

- If an ASO was entered before the error the device remains entered in the ASO awaiting ASO read or a command write.
- If an erase was suspended before the error the device returns to the erase suspended state awaiting flash array read or a command write.
- Otherwise, the device will be in standby state awaiting flash array read or a command write.

5.6.1 Embedded operation error

If an error occurs during an embedded operation (program, erase, blank check, or password unlock) the device (EAC) remains busy. The RY/BY# output remains LOW, data polling status continues to be overlaid on all address locations, and the status register shows ready with valid status bits. The device remains busy until the error status is detected by the host system status monitoring and the error status is cleared.

During embedded algorithm error status the data polling status will show the following:

- DQ7 is the inversion of the DQ7 bit in the last word loaded into the write buffer or last word of the password in the case of the password unlock command. DQ7 = 0 for an erase or blank check failure
- DQ6 continues to toggle
- DQ5 = 1; Failure of the embedded operation
- DQ4 is RFU and should be treated as don’t care (masked)
- DQ3 = 1 to indicate embedded sector erase in progress
- DQ2 continues to toggle, independent of the address used to read status
- DQ1 = 0; Write buffer abort error
- DQ0 is RFU and should be treated as don’t care (masked)

During embedded algorithm error status the Status Register will show the following:

- SR[7] = 1; Valid status displayed
- SR[6] = X; May or may not be erase suspended during the EA error
- SR[5] = 1 on erase or blank check error; else = 0
- SR[4] = 1 on program or password unlock error; else = 0
- SR[3] = 0; Write buffer abort
- SR[2] = 0; Program suspended
- SR[1] = 0; Protected sector
- SR[0] = X; RFU, treat as don’t care (masked)

When the embedded algorithm error status is detected, it is necessary to clear the error status in order to return to normal operation, with RY/BY# HIGH, ready for a new read or command write. The error status can be cleared by writing:

- Reset command
- Status Register Clear command

Commands that are accepted during embedded algorithm error status are:

- Status Register Read
- Reset command
- Status Register Clear command

5.6.2 Protection error

If an embedded algorithm attempts to change data within a protected area (program, or erase of a protected sector or OTP area) the device (EAC) goes busy for a period of 20 to 100 µs then returns to normal operation. During the busy period the RY/BY# output remains LOW, data polling status continues to be overlaid on all address locations, and the status register shows not ready with invalid status bits (SR[7] = 0).

During the protection error status busy period the data polling status will show the following:

- DQ7 is the inversion of the DQ7 bit in the last word loaded into the write buffer. DQ7 = 0 for an erase failure
- DQ6 continues to toggle, independent of the address used to read status
- DQ5 = 0; to indicate no failure of the embedded operation during the busy period
- DQ4 is RFU and should be treated as don't care (masked)
- DQ3 = 1 to indicate embedded sector erase in progress
- DQ2 continues to toggle, independent of the address used to read status
- DQ1 = 0; Write buffer abort error
- DQ0 is RFU and should be treated as don't care (masked)

Commands that are accepted during the protection error status busy period are:

- Status Register Read

When the busy period ends the device returns to normal operation, the data polling status is no longer overlaid, RY/BY# is High, and the status register shows ready with valid status bits. The device is ready for flash array read or write of a new command.

After the protection error status busy period the Status Register will show the following:

- SR[7] = 1; Valid status displayed
- SR[6] = X; May or may not be erase suspended after the protection error busy period
- SR[5] = 1 on erase error, else = 0
- SR[4] = 1 on program error, else = 0
- SR[3] = 0; Program not aborted
- SR[2] = 0; No Program in suspension
- SR[1] = 1; Error due to attempting to change a protected location
- SR[0] = X; RFU, treat as don't care (masked)

Commands that are accepted after the protection error status busy period are:

- Any command

5.6.3 Write buffer abort

If an error occurs during a Write to Buffer command the device (EAC) remains busy. The RY/BY# output remains LOW, data polling status continues to be overlaid on all address locations, and the status register shows ready with valid status bits. The device remains busy until the error status is detected by the host system status monitoring and the error status is cleared.

During write to buffer abort (WBA) error status the Data Polling status will show the following:

- DQ7 is the inversion of the DQ7 bit in the last word loaded into the write buffer
- DQ6 continues to toggle, independent of the address used to read status
- DQ5 = 0; to indicate no failure of the programming operation. WBA is an error in the values input by the Write to Buffer command before the programming operation can begin
- DQ4 is RFU and should be treated as don't care (masked)
- DQ3 is don't care after program operation as no erase is in progress. If the Write Buffer Program operation was started after an erase operation had been suspended then DQ3 = 1. If there was no erase operation in progress then DQ3 is a don't care and should be masked.
- DQ2 does not toggle after program operation as no erase is in progress. If the Write Buffer Program operation was started after an erase operation had been suspended then DQ2 will toggle in the sector where the erase operation was suspended and not in any other sector. If there was no erase operation in progress then DQ2 is a don't care and should be masked.
- DQ1 = 1: Write buffer abort error
- DQ0 is RFU and should be treated as don't care (masked)

During embedded algorithm error status the Status Register will show the following:

- SR[7] = 1; Valid status displayed
- SR[6] = X; May or may not be erase suspended during the WBA error status
- SR[5] = 0; Erase successful
- SR[4] = 1; Programming related error
- SR[3] = 1; Write buffer abort
- SR[2] = 0; No Program in suspension
- SR[1] = 0; Sector not locked during operation
- SR[0] = X; RFU, treat as don't care (masked)

When the WBA error status is detected, it is necessary to clear the error status in order to return to normal operation, with RY/BY# HIGH, ready for a new read or command write. The error status can be cleared and device returned to normal operation by writing:

- Write Buffer Abort Reset command
  - Clears the status register and returns to normal operation
- Status Register Clear command

Commands that are accepted during embedded algorithm error status are:

- Status Register Read
- Write Buffer Abort Reset command
- Status Register Clear command

5.7 Embedded Algorithm Performance table

Table 16 Embedded algorithm characteristics (–40°C to +85°C)

Parameter		Typ[29]	Max[30]	Unit	Comments
Sector Erase time 128 kbyte		275	1100	ms	Includes pre-programming prior to erasure[32]
Single Word Programming time[33]		125	400	µs	
Buffer Programming time	2-byte[33]	125	750	µs	
	32-byte[33]	160	750		
	64-byte[33]	175	750		
	128-byte[33]	198	750		
	256-byte[33]	239	750		
	512-byte	340	750		
Effective Write Buffer Program operation per word	512-byte	1.33	–	µs	
Sector Programming time 128 kB (full Buffer Programming)		108	192	ms	Note 34
Erase Suspend/Erase Resume (t_{ESL})		–	40	µs	
Program Suspend/Program Resume (t_{PSL})		–	40	µs	
Erase Resume to next Erase Suspend (t_{ERS})		100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for Erase to progress to completion.
Program Resume to next Program Suspend (t_{PRS})		100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for Program to progress to completion.
Blank Check		6.2	8.5	ms	
NOP (Number of Program-operations, per line)		–	256		

Notes
29. Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 10,000 cycle, and a random data pattern.
30. Under worst case conditions of 90°C, V_{CC} = 2.70 V, 100,000 cycles, and a random data pattern.
31. Effective write buffer specification is based upon a 512-byte write buffer operation.
32. In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 0000h before Sector and Chip erasure.
33. Not 100% tested.
34. System-level overhead is the time required to execute the bus-cycle sequence for the program command. See **Table 41** for further information on command definitions.

Table 17 Embedded algorithm characteristics (–40°C to +105°C)

Parameter		Typ[35]	Max[36]	Unit	Comments
Sector Erase time 128 kbyte		275	1100	ms	Includes pre-programming prior to erasure[38]
Single Word Programming time[39]		125	400	µs	
Buffer Programming time	2-byte[39]	150	1050	µs	
	32-byte[39]	200	1050		
	64-byte[39]	220	1050		
	128-byte[39]	250	1050		
	256-byte[39]	320	1050		
	512-byte	420	1050		
Effective Write Buffer Program operation per word	512-byte	1.64	–	µs	
Sector Programming time 128 kB (full Buffer Programming)		108	269	ms	Note 40
Erase Suspend/Erase Resume (t_{ESL})		–	50	µs	
Program Suspend/Program Resume (t_{PSL})		–	50	µs	
Erase Resume to next Erase Suspend (t_{ERS})		100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for Erase to progress to completion.
Program Resume to next Program Suspend (t_{PRS})		100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for Program to progress to completion.
Blank Check		7.6	9.0	ms	
NOP (Number of Program-operations, per line)		–	1 per 16 word		

Notes
35. Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 10,000 cycle, and a random data pattern.
36. Under worst case conditions of 105°C, V_{CC} = 2.70 V, 100,000 cycles, and a random data pattern.
37. Effective write buffer specification is based upon a 512-byte write buffer operation.
38. In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 0000h before Sector and Chip erasure.
39. Not 100% tested.
40. System-level overhead is the time required to execute the bus-cycle sequence for the program command. See **Table 41** for further information on command definitions.

5.7.1 Command State Transitions

Table 18 Read Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Blank Check	CFI Entry
	Address	RA	xh	x555h	x555h	x555h	(SA)555h	(SA)55h
	Data	RD	xF0h	x70h	x71h	xAAh	x33h	x98h
READ	–	READ	READ	READSR (READ)	READ	READUL1	–	CFI
	Read Protect = False						BLCK	
READSR	–	(return)	–	–	–	–	–	–

Table 19 Read Unlock Command State Transition

Current State	Command and Condition	Read	Status Register Read Enter	Unlock 2	Word Program Entry	Write to Buffer Enter	Erase Enter	ID (Auto-select) Entry	SSR Entry	Lock Register Entry	Password ASO Entry	PPB Entry	PPB Lock Entry	DYB ASO Entry
	Address	RA	x555h	x2AAh	x555h	(SA)xh	x555h	(SA)555h	(SA)555h	x555h	x555h	x555h	x555h	x555h
	Data	RD	x70h	x55h	xA0h	x25h	x80h	x90h	x88h	x40h	x60h	xC0h	x50h	xE0h
READUL1	–	READUL1	READSR (READ)	READUL2	–	–	–	–	–	–	–	–	–	–
READUL2	Read Protect = True	READUL2	READSR (READ)	–	–	–	–	CFI	–	–	PP	–	–	–
	Read Protect = False				PG1	WB	ER		SSR	LR			PPBLB	DYB
	Read Protect = False and LR(8) = 0											PPB		

Table 20 Erase State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Unlock 2	Chip Erase Start	Sector Erase Start	Erase Suspend Enhanced Method [41]
	Address	RA	xh	x555h	x555h	x555h	x2AAh	x555h	(SA)xh	xh
	Data	RD	xF0h	x70h	x71h	xAAh	x55h	x10h	x30h	xB0h
ER	–	ER	–	READSR (READ)	--	ERUL1	–	–	–	–
ERUL1	–	ERUL1	–	READSR (READ)	–	–	ERUL2	–	–	–
ERUL2	–	ERUL2	–	READSR (READ)	–	–	–	CER	SER	–
CER [42]	–	CER	–	ERSR (CER)	–	–	–	–	–	–
SER [42]	SR(7) = 0	SER	–	ERSR (SER)	–	–	–	–	–	ESR (ES)
	SR(7) = 1		READ		READ					
BLCK [42]	SR(7) = 0	BLCK	–	ERSR (BLCK)	–	–	–	–	–	–
	SR(7) = 1		READ		READ					
ERSR	–	(return)	–	–	–	–	–	–	–	–

Notes
41.Also known as Erase Suspend/Program Suspend Legacy Method.
42.State will automatically move to READ state at the completion of the operation.

Table 21 Erase Suspend State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Sector Erase Start
	Address	RA	xh	x555h	x555h	x555h	(SA)xh
	Data	RD	xF0h	x70h	x71h	xAAh	x30h
ESR [43]	–	ESR	–	ERSR (ESR)	–	–	–
ES	SR(7) = 0	ES	ES	ESSR (ES)	ES	ESUL1	–
	SR(7) = 1						SER
ESSR	–	(return)	–	–	–	–	–

Table 22 Erase Suspend Unlock State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Unlock 1	Word Program Entry	Write to Buffer Enter	Write-to-Buffer-Abort Reset Start	Erase Resume Enhanced Method [44]	DYB ASO Entry	NOT a valid "Write-to-Buffer-Abort Reset" Command			
	Address	RA	xh	x555h	x2AAh	x555h	(SA)xh	x555h	xh	x555h	NOT x555h	xh	NOT x2AAh	xh
	Data	RD	xF0h	x70h	x55h	xA0h	x25h	xF0h	x30h	xE0h	xh	NOT xF0h	xh	NOT x55h
ESUL1	–	ESUL1	–	ESSR (ES)	ESUL2	–	–	–	–	–	–	–	–	–
	SR(3) = 1												ESPG	ESPG
	DQ(1) = 1													
ESUL2	–	ESUL2	ES	ESSR (ES)	–	ESPG1	ES_WB	–	SER	–	–	–	–	–
	Read Protect = False									ESDYB				
	SR(3) = 1		–					ES		–	ESPG	ESPG		
	DQ(1) = 1													

Table 23 Erase Suspend - DYB State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	DYB Set/Clear Entry	Password Word Count
	Address	RA	xh	x555h	x555h	xh	xh	xh	xh
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h	x03h
ESDYB	–	ESDYB	ES	ESSR (ESDYB)	ESDYB	ESDYBEXT	–	ESDYBSET	–
ESDYBSET	–	ESDYBSET	–	–	–	–	–	–	–
ESDYBEXT	–	ESDYBEXT	–	–	–	–	ES	–	ES

Notes

43. State will automatically move to ES state by t_{ESL}.
44. Also known as Erase Resume/Program Resume Legacy Method.

Table 24 Erase Suspend - Program Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Erase Suspend Enhanced Method [45]	ProgramSuspend Enhanced Method	Write Data
	Address	RA	xh	x555h	x555h	x555h	xh	xh	xh
	Data	RD	xF0h	x70h	x71h	xAAh	xB0h	x51h	xh
ES_WB	WC > 256 or SA ≠ SA	ES_WB	–	–	–	–	–	–	ESPG
	WC ≤ 256 and SA = SA								ES_WB_D
ES_WB_D	WC < 0 or Write Buffer ≠ Write Buffer	ES_WB_D	–	–	–	–	–	–	ESPG
	WC > 0 and Write Buffer = Write Buffer								ES_WB_D
ESPG1	–	ESPG1	–	–	–	–	–	–	ESPG
ESPG	SR(7) = 0	ESPG	–	ESPGSR (ESPG)	–	–	ESPSR (ESPG)	ESPSR (ESPG)	ESPG
	SR(7) = 1		ES		ES	ESUL1			
ESPGSR	–	(return)	–	–	–	–	–	–	(return)

Table 25 Erase Suspend - Program Suspend Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Unlock 2	Erase Resume Enhanced Method [46]	Program Resume Enhanced Method
	Address	RA	xh	x555h	x555h	x555h	x2AAh	xh	xh
	Data	RD	xF0h	x70h	x71h	xAAh	x55h	x30h	x50h
ESPSR [47]	–	ESPSR	–	ESPGSR (ESPSR)	–	–	–	–	–
ESPS	–	ESPS	ESPS	ESPSSR (ESSP)	ESPS	ESPSUL1	–	ESPG	ESPG
ESPSSR	–	(return)	–	–	–	–	–	–	–
ESPSUL1	–	ESPSUL1	–	ESPSSR (ESPS)	–	–	ESPSUL2	–	–
ESPSUL2	–	ESPSUL2	–	ESPSSR (ESPS)	–	–	–	ESPG	ESPG

Notes
45. Also known as Erase Suspend/Program Suspend Legacy Method.
46. Also known as Erase Resume/Program Resume Legacy Method.
47. State will automatically move to ESPS state by t_{PSL}.

Table 26 Program State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Program Buffer to flash (confirm)	Erase Suspend Enhanced Method [48]	Program Suspend Enhanced Method	Write Data
	Address	RA	xh	x555h	x555h	x555h	(SA)xh	xh	xh	xh
	Data	RD	xF0h	x70h	x71h	xAAh	x29h	xB0h	x51h	xh
WB	WC > 256 or SA ≠ SA	WB	–	–	–	–	––	–	–	PG
	WC ≤ 256 and SA = SA									WB_D
WB_D	Write Buffer ≠ Write Buffer	WB_D	–	–	–	–	–	–	–	PG
	WC = 0									PBF
	WC > 0 and Write Buffer = Write Buffer									WB_D
PBF	–	–	–	–	–	–	PG	–	–	PG
PG1	–	PG1	–	–	–	–	–	–	–	PG
PG [49]	SR(7) = 0	PG	–	PGSR (PG)	–	–	–	PSR (PG)	PSR (PG)	PG
	SR(7) = 1		READ		READ	WBUL1		–	–	
	SR(7) = 1 and SR(1) = 0									

Table 27 Program Unlock State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Unlock 2	NOT a valid "Write-to-Buffer-Abort Reset" Command			
	Address	RA	xh	x555h	x2AAh	NOT x555h	xh	NOT x2AAh	xh
	Data	RD	xF0h	x70h	x55h	xh	NOT xF0h	xh	NOT x55h
WBUL1	–	WBUL1	–	–	WBUL2	–	–	–	–
	SR(3) = 1							PG	PG
	DQ(1) = 1								
WBUL2	–	WBUL2	READ	–	–	–	–	–	–
	SR(3) = 1					PG	PG		
	DQ(1) = 1								
PGSR	–	(return)	–	–	–	–	–	–	–

Notes
48. Also known as Erase Suspend/Program Suspend Legacy Method.
49. State will automatically move to READ state at the completion of the operation.

Table 28 Program Suspend State Command Transition

Current State	Command and Condition	Read	Status Register Read Enter	Status Register Clear	Erase Resume Enhanced Method [50]	Program Resume Enhanced Method
	Address	RA	x555h	x555h	xh	xh
	Data	RD	x70h	x71h	x30h	x50h
PSR [51]	–	PSR	PGSR (PSR)	–	–	–
PS	–	PS	PSSR (PS)	PS	PG	PG
PSSR	–	(return)	–	–	–	–

Table 29 Lock Register State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	PPB Lock Bit Set Entry	Password Word Count
	Address	RA	xh	x555h	x555h	xh	xh	xh	Xh
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h	x03h
LR	–	LR	READ	LRSR (LR)	LR	LREXT	–	LRPG1	–
LRPG1	–	LRPG1	–	–	–	–	–	–	–
LRPG	–	LRPG	–	LRSR (LRPG)	–	–	–	–	–
LRSR	–	(return)	–	–	–	–	–	–	–
LREXT	–	LREXT	–	–	–	–	READ	–	READ

Table 30 CFI State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear
	Address	RA	xh	x555h	x555h
	Data	RD	xF0h	x70h	x71h
CFI	–	CFI	READ	CFISR (CFI)	CFI
CFISR	–	(return)	–	–	–

Table 31 Secure Silicon Sector State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1
	Address	RA	xh	x555h	x555h	x555h
	Data	RD	xF0h	x70h	x71h	xAAh
SSR	–	SSR	READ	SSRSR (SSR)	SSR	SSRUL1

Table 32 Secure Silicon Sector Unlock State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Unlock 2	Word Program Entry	Write to Buffer Enter	Command Set Exit Entry	NOT a valid "Write-to-Buffer-Abort Reset" Command			
	Address	RA	xh	x555h	x2AAh	x555h	(SA)xh	x555h	NOT x555h	xh	NOT x2AAh	xh
	Data	RD	xF0h	x70h	x55h	xA0h	x25h	x90h	xh	NOT xF0h	xh	NOT x55h
SSRUL1	–	SSRUL1	READ	SSRSR (SSR)	SSRUL2	–	–	–	–	–	–	–
	DQ(1) = 1										SSRPG	SSRPG
	SR(3) = 1											
SSRUL2	–	SSRUL2	SSR	–	–	SSRPG1	SSR_WB	SSREXT	–	–	–	–
	DQ(1) = 1								SSRPG	SSRPG		
	SR(3) = 1											

Notes
50.Also known as Erase Resume/Program Resume Legacy Method.
51.State will automatically move to PS state by t_{PSL}.

Table 33 Secure Silicon Sector Program State Command Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Command Set Exit
	Address	RA	xh	x555h	x555h	x555h	xh
	Data	RD	xF0h	x70h	x71h	xAAh	x00h
SSRPG1	–	SSRPG1	–	–	SSRPG1	–	–
SSR_WB	WC > 256 or SA ≠ SA	SSR_WB	–	–	–	–	–
	WC ≤ 256 and SA = SA						
SSR_WB_D	WC < 0 or Write Buffer ≠ Write Buffer	SSR_WB_D	–	–	–	–	–
	WC > 0 and Write Buffer = Write Buffer						
SSRPG	SR(7) = 0	SSRPG	–	SSRSR (SSRPG)	–	–	–
	SR(7) = 1				SSR		
	SR(7) = 1 and DQ(1) = 0		READ				
	DQ(1) = 1		–		–	SSRUL1	
	SR(3) = 1						
SSRSR	–	(return)	–	–	–	–	–
SSREXT	–	SSREXT	–	SSRSR (SSR)	–	–	READ

Table 34 Password Protection Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Password ASO Unlock Enter	Password ASO Unlock Start	Command Set Exit Entry	Command Set Exit	Program Entry	Password Word Count
	Address	RA	xh	x555h	x555h	0h	0h	xh	xh	xh	Xh
	Data	RD	xF0h	x70h	x71h	x25h	x29h	x90h	x00h	xA0h	x03h
PP	–	PP	READ	PPSR (PP)	PP	PPWB25	–	PPEXT	–	PPPG1	–
PPWB25	–	PPWB25	–	–	–	–	–	–	–	–	PPD
PPD	WC > 0	PPD	–	–	–	–	–	–	–	–	–
	WC ≤ 0	-					PPPG				
PPPG1	–	PPPG1	–	–	–	–	–	–	–	–	–
PPPG	–	PPPG	–	PPSR (PPPG)	–	–	–	–	–	–	–
PPSR	–	(return)	–	–	–	–	–	–	–	–	–
PPEXT	–	PPEXT	–	–	–	–	–	–	READ	–	–

Table 35 Non-Volatile Protection Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	Program Entry	DYB Set Start	All PPB Erase Enter	All PPB Erase Start
	Address	RA	xh	x555h	x555h	xh	xh	xh	(SA)xh	Xh	0h
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h	x00h	x80h	x30h
PPB	–	PPB	READ	PPBSR (PPB)	PPB	PPBEXT	–	PPBPG1	–	PPBPG1	–
PPBPG1	–	PPBPG1	READ	–	–	–	PPBPG	–	PPB	–	PPBER
PPBPG	SR(7) = 0	PPBPG	–	PPBSR (PPBPG)	–	–	–	–	–	–	–
	SR(7) = 1		READ		READ						
PPBER	SR(7) = 0	PPBER	–	PPBSR (PPBER)	–	–	–	–	–	–	–
	SR(7) = 1		READ		READ						
PPBSR	–	(return)	–	–	–	–	–	–	–	–	–
PPBEXT	–	PPBEXT	–	–	–	–	READ	-	-	–	–

Table 36 PPB Lock Bit Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	Program Entry
	Address	RA	xh	x555h	x555h	xh	xh	xh
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h
PPBLB	–	PPBLB	READ	PPBLBSR (PPBLB)	PPBLB	PPBLBEXT	–	PPBLBSET
PPBLBSR	–	(return)	–	–	–	–	–	–
PPBLBSET	–	PPBLBSET	–	–	–	–	PPBLB	–
	LR(2) = 0 and LR(5) = 0							
PPBLBEXT	–	PPBLBEXT	–	–	–	–	READ	–

Table 37 Volatile Sector Protection Command State Transition

Current State	Command and Condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	Program Entry	DYB Set Start	DYB Clear Start
	Address	RA	xh	x555h	x555h	xh	xh	xh	(SA)xh	(SA)xh
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h	x00h	x01h
DYB	–	DYB	READ	DYBSR (DYB)	DYB	DTBEXT	–	DYBSET	–	–
DYBSR	–	(return)	–	–	–	–	–	–	–	–
DYBSET	–	DYBSET	–	–	–	–	–	–	DYB	DYB
DYBEXT	–	DYBEXT	–	–	–	–	READ	–	–	–

Table 38 State Transition definitions

Current state	Command transition	Definition
BLCK	Table 20	Blank Check
CER	Table 20	Chip Erase Start
CFI	Table 30	ID (Autoselect)
CFISR	Table 30	ID (Autoselect) - Status Register Read
DYB	Table 37	DYB ASO
DYBEXT	Table 37	DYB ASO - Command Exit
DYBSET	Table 37	DYB ASO - Set
DYBSR	Table 37	DYB ASO - Status Register Read
ER	Table 20	Erase Enter
ERSR	Table 20	Erase - Status Register Read
ERUL1	Table 20	Erase - Unlock Cycle 1
ERUL2	Table 20	Erase - Unlock Cycle 2
ES	Table 21	Erase Suspended
ESDYB	Table 23	Erase Suspended - DYB ASO
ESDYBEXT	Table 23	Erase Suspended - DYB Command Exit
ESDYBSET	Table 23	Erase Suspended - DYB Set/Clear
ESPG	Table 24	Erase Suspended - Program
ESPGSR	Table 24	Erase Suspended - Program - Status Register Read
ESPG1	Table 24	Erase Suspended - Word Program
ESPS	Table 25	Erase Suspended - Program Suspended
ESPSR	Table 25	Erase Suspended - Program Suspend
ESPSSR	Table 25	Erase Suspended - Program Suspend - Status Register Read
ESPSUL1	Table 25	Erase Suspended - Program Suspend - Unlock 1
ESPSUL2	Table 25	Erase Suspended - Program Suspend - Unlock 2
ESR	Table 21	Erase Suspend Request
ESSR	Table 21	Erase Suspended - Status Register Read
ESUL1	Table 22	Erase Suspended - Unlock Cycle 1
ESUL2	Table 22	Erase Suspended - Unlock Cycle 2
ES_WB	Table 24	Erase Suspended - Write to Buffer
ES_WB_D	Table 24	Erase Suspended - Write to Buffer Data
LR	Table 29	Lock Register
LREXT	Table 29	Lock Register - Command Exit
LRPG	Table 29	Lock Register - Program
LRPG1	Table 29	Lock Register - Program Start
LRSR	Table 29	Lock Register - Status Register Read
PBF	Table 26	Page Buffer Full
PG	Table 26	Program
PGSR	Table 27	Program - Status Register Read
PG1	Table 26	Word Program

Table 38 State Transition definitions (Continued)

Current state	Command transition	Definition
PP	Table 34	Password ASO
PPB	Table 35	PPB
PPBER	Table 35	PPB - Erase
PPBEXT	Table 35	PPB - Command Exit
PPBLB	Table 36	PPB Lock Bit
PPBLBEXT	Table 36	PPB Lock Bit - Command Exit
PPBLBSET	Table 36	PPB Lock Bit - Set
PPBLBSR	Table 36	PPB Lock Bit - Status Register Read
PPBPG	Table 35	PPB - Program
PPBPG1	Table 35	PPB - Program Request
PPBSR	Table 35	PPB - Status Register Read
PPD	Table 34	Password ASO - Data
PPEXT	Table 34	Password ASO - Command Exit
PPPG	Table 34	Password ASO - Program
PPPG1	Table 34	Password ASO - Program Request
PPSR	Table 34	Password ASO - Status Register Read
PS	Table 28	Program Suspended
PSR	Table 28	Program Suspend Request
PSSR	Table 28	Program Suspended - Status Register Read
PPWB25	Table 34	Password ASO - Unlock
READ	Table 18	Read Array
READSR	Table 18	Read Status Register
READUL1	Table 19	Read - Unlock Cycle 1
READUL2	Table 19	Read - Unlock Cycle 2
SER	Table 20	Sector Erase Start
SSR	Table 31	Secure Silicon
SSREXT	Table 33	Secure Silicon - Command Exit
SSRPG	Table 33	Secure Silicon - Program
SSRPG1	Table 33	Secure Silicon - Word Program
SSRSR	Table 33	Secure Silicon - Status Register Read
SSRUL1	Table 32	Secure Silicon - Unlock Cycle 1
SSRUL2	Table 32	Secure Silicon - Unlock Cycle 2
SSR_WB	Table 33	Secure Silicon - Write to Buffer
SSR_WB_D	Table 33	Secure Silicon - Write to Buffer - Write Data
WB	Table 26	Write to Buffer
WBUL1	Table 27	Write Buffer - Unlock Cycle 1
WBUL2	Table 27	Write Buffer - Unlock Cycle 2
WB_D	Table 26	Write to Buffer Write Data

6 Data integrity

6.1 Erase endurance

Table 39 Erase endurance

Parameter	Minimum	Unit
Program/Erase cycles per main Flash array sectors	100K	P/E cycle
Program/Erase cycles per PPB array or non-volatile register array	100K	P/E cycle

6.2 Data retention

Table 40 Data retention

Parameter	Test conditions	Minimum time	Unit
Data retention time	10K program/erase cycles	20	Years
	100K program/erase cycles	2	Years

Contact Infineon Sales or an FAE representative for additional information on the data integrity. An application note is available at **https://www.infineon.com/cms/en/product/memories/nor-flash/#!documents**.

Note
52. Each write command to a non-volatile register causes a P/E cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not P/E cycled.

7 Software interface reference

7.1 Command summary

Table 41 Command definitions

Command Sequence [53]		Cycles	Bus Cycles [54, 55, 56, 57]													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read[58]		1	RA	RD												
Reset/ASO Exit[59, 60]		1	XXX	F0												
Status Register Read		2	555	70	XXX	RD										
Status Register Clear		1	555	71												
Word Program		4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer		6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
Program Buffer to Flash (confirm)		1	SA	29												
Write-to-Buffer-Abort Reset[61]		3	555	AA	2AA	55	555	F0								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend/Program Suspend Legacy Method[62]		1	XXX	B0												
Erase Suspend Enhanced Method																
Erase Resume/Program Resume Legacy Method[63]		1	XXX	30												
Erase Resume Enhanced Method																
Program Suspend Enhanced Method		1	XXX	51												
Program Resume Enhanced Method		1	XXX	50												
Blank Check		1	(SA) 555	33												
ID-CFI (Autoselect) ASO	ID (Autoselect) Entry	3	555	AA	2AA	55	(SA) 555	90								
	CFI Enter[64]	1	(SA) 55	98												
	ID-CFI Read	1	RA	RD												
	Reset/ASO Exit [59, 60]	1	XXX	F0												
Secure Silicon Region Command Definitions																
Secure Silicon Region (SSR) ASO	SSR Entry	3	555	AA	2AA	55	(SA) 555	88								
	Read[58]	1	RA	RD												
	Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
	Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
	Program Buffer to Flash (confirm)	1	SA	29												
	Write-to-Buffer-Abort Reset[61]	3	555	AA	2AA	55	555	F0								
	SSR Exit[61]	4	555	AA	2AA	55	555	90	XX	0						
	Reset/ASO Exit[59, 60]	1	XXX	F0												

Table 41 Command definitions (Continued)

	Command Sequence [53]	Cycles	Bus Cycles [54, 55, 56, 57]													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Command Set Definitions																
Lock Register ASO	Lock Register Entry	3	555	AA	2AA	55	555	40								
	Program[65]	2	XXX	A0	XXX	PD										
	Read[65]	1	0	RD												
	Command Set Exit[60, 66]	2	XXX	90	XXX	0										
	Reset/ASO Exit [59, 60]	1	XXX	F0												
Password Protection Command Set Definitions																
Password ASO	Password ASO Entry	3	555	AA	2AA	55	555	60								
	Program[67]	2	XXX	A0	PWA x	PWDx										
	Read[68]	4	0	PWD0	1	PWD1	2	PWD2	3	PWD3						
	Unlock	7	0	25	0	3	0	PWD0	1	PWD1	2	PWD2	3	PWD3	0	29
	Command Set Exit[60, 66]	2	XXX	90	XXX	0										
	Reset/ASO Exit[59, 60]	1	XXX	F0												
Non-Volatile Sector Protection Command Set Definitions																
PPB (Non-Volatile Sector Protection)	PPB Entry	3	555	AA	2AA	55	555	C0								
	PPB Program[69]	2	XXX	A0	SA	0										
	All PPB Erase[69]	2	XXX	80	0	30										
	PPB Read[69]	1	SA	RD (0)												
	Command Set Exit[60, 66]	2	XXX	90	XXX	0										
	Reset/ASO Exit[59, 60]	1	XXX	F0												
Global Non-Volatile Sector Protection Freeze Command Set Definitions																
PPB Lock Bit	PPB Lock Entry	3	555	AA	2AA	55	555	50								
	PPB Lock Bit Cleared	2	XXX	A0	XXX	0										
	PPB Lock Status Read[69]	1	XXX	RD (0)												
	Command Set Exit[60, 66]	2	XXX	90	XXX	0										
	Reset/ASO Exit[60]	1	XXX	F0												
Volatile Sector Protection Command Set Definitions																
DYB (Volatile Sector Protection) ASO	DYB ASO Entry	3	555	AA	2AA	55	555	E0								
	DYB Set[69]	2	XXX	A0	SA	0										
	DYB Clear[69]	2	XXX	A0	SA	1										
	DYB Status Read[69]	1	SA	RD (0)												
	Command Set Exit[60, 66]	2	XXX	90	XXX	0										
	Reset/ASO Exit[60]	1	XXX	F0												
Command Set Definitions ECC																
ECC ASO	ECC ASO Entry	3	555	AA	2AA	55	555	75								
	ECC Status Read	1	RA	RD												
	Command Set Exit[60, 66]	1	XXX	F0												

Legend:
X = Don't care.
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed.
PD = Data to be programmed at location PA.
SA = Address of the sector selected. Address bits A_{MAX}–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same Line.
WC = Word Count is the number of write buffer locations to load minus 1.
PWAx = Password address for word0 = 00h, word1 = 01h, word2 = 02h, and word3 = 03h.
PWDx = Password data word0, word1, word2, and word3.

Notes
53. See **Table 49** for description of bus operations.
54. All values are in hexadecimal.
55. Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.
56. Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, WC and PWD.
57. Address bits A_{MAX}–A11 are don't cares for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).
58. No unlock or command cycles required when reading array data.
59. The Reset command is required to return to reading array data when device is in the ID-CFI (autoselect) mode, or if DQ5 goes High (while the device is providing status data).
60. If any of the Entry commands was issued, an Exit command must be issued to reset the device into read mode.
61. Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. IMPORTANT: the full command sequence is required if resetting out of ABORT.
62. The system can read and program/program suspend in non-erasing sectors, or enter the ID-CFI ASO, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
63. The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.
64. Command is valid when device is ready to read array data or when device is in ID-CFI (autoselect) mode.
65. All Lock Register bits are one-time programmable. The program state = 0 and the erase state = 1. Also, both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation aborts and returns the device to read mode. Lock Register bits that are reserved for future use are undefined and may be 0's or 1's.
66. The Exit command returns the device to reading the array.
67. For PWDx, only one portion of the password can be programmed per each A0 command. Portions of the password must be programmed in sequential order (PWD0–PWD3).
68. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
69. Protected State = 00h, Unprotected State = 01h. The sector address for DYB set, DYB clear, or PPB Program command may be any location within the sector - the lower order bits of the sector address are don't care.

7.2 Device ID and Common Flash Interface (ID-CFI) ASO Map

The Device ID portion of the ASO (word locations 0h to 0Fh) provides manufacturer ID, device ID, Sector Protection State, and basic feature set information for the device.

ID-CFI Location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go High before the read and return Low to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

For additional information see **"ID-CFI ASO"** on page 33.

Table 42 ID (Autoselect) address map

Description	Address	Read data
Manufacture ID	(SA) + 0000h	0001h
Device ID	(SA) + 0001h	227Eh
Protection verification	(SA) + 0002h	Sector Protection State (1= Sector protected, 0 = Sector unprotected). This protection state is shown only for the SA selected when entering ID-CFI ASO. Reading other SA provides undefined data. To read a different SA protection state ASO exit command must be used and then enter ID-CFI ASO again with the new SA.
Indicator Bits	(SA) + 0003h	DQ15–DQ08 = 1 (Reserved) DQ7 - Factory Locked Secure Silicon Region 1 = Locked, 0 = Not Locked DQ6 - Customer Locked Secure Silicon Region 1 = Locked 0 = Not Locked DQ5 = 1 (Reserved) DQ4 - WP# Protects 0 = lowest address Sector 1 = highest address Sector DQ3–DQ0 = 1 (Reserved)
RFU	(SA) + 0004h	Reserved
	(SA) + 0005h	Reserved
	(SA) + 0006h	Reserved
	(SA) + 0007h	Reserved
	(SA) + 0008h	Reserved
	(SA) + 0009h	Reserved
	(SA) + 000Ah	Reserved
	(SA) + 000Bh	Reserved

Table 42 ID (Autoselect) address map (Continued)

Description	Address	Read data
Lower software bits	(SA) + 000Ch	Bit 0 - Status Register Support 1 = Status Register Supported 0 = Status Register not supported Bit 1 - DQ polling Support 1 = DQ bits polling supported 0 = DQ bits polling not supported Bit 3–2 - Command Set Support 11 = reserved 10 = reserved 01 = Reduced Command Set 00 = Classic Command set Bits 4–15 - Reserved = 0
Upper software bits	(SA) + 000Dh	Reserved
Device ID	(SA) + 000Eh	2228h = 1 Gb 2223h = 512 Mb 2222h = 256 Mb 2221h = 128 Mb
Device ID	(SA) + 000Fh	2201h

Table 43 CFI query identification string

Word address	Data	Description
(SA) + 0010h (SA) + 0011h (SA) + 0012h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
(SA) + 0013h (SA) + 0014h	0002h 0000h	Primary OEM Command Set
(SA) + 0015h (SA) + 0016h	0040h 0000h	Address for Primary Extended Table
(SA) + 0017h (SA) + 0018h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
(SA) + 0019h (SA) + 001Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 44 CFI system interface string

Word address	Data	Description
(SA) + 001Bh	0027h	V_{CC} Min. (erase/program) (D7–D4: volts, D3–D0: 100 mV)
(SA) + 001Ch	0036h	V_{CC} Max. (erase/program) (D7–D4: volts, D3–D0: 100 mV)
(SA) + 001Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
(SA) + 001Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
(SA) + 001Fh	0008h	Typical timeout per single word write 2^N µs
(SA) + 0020h	0009h	Typical timeout for max multi-byte program, 2^N µs (00h = not supported)
(SA) + 0021h	0008h	Typical timeout per individual block erase 2^N ms
(SA) + 0022h	0012h (1 Gb) 0011h (512 Mb) 0010h (256 Mb) 000Fh (128 Mb)	Typical timeout for full chip erase 2^N ms (00h = not supported)
(SA) + 0023h	0001h	Max. timeout for single word write 2^N times typical
(SA) + 0024h	0002h	Max. timeout for buffer write 2^N times typical
(SA) + 0025h	0003h	Max. timeout per individual block erase 2^N times typical
(SA) + 0026h	0003h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 45 CFI device geometry definition

Word Address	Data	Description
(SA) + 0027h	001Bh (1 Gb) 001Ah (512 Mb) 0019h (256 Mb) 0018h (128 Mb)	Device Size = 2^N byte
(SA) + 0028h	0001h	Flash Device Interface Description 0 = ×8-only, 1 = ×16-only, 2 = ×8/×16 capable
(SA) + 0029h	0000h	
(SA) + 002Ah	0009h	Max. number of byte in multi-byte write = 2^N (00 = not supported)
(SA) + 002Bh	0000h	
(SA) + 002Ch	0001h	Number of Erase Block Regions within device 1 = Uniform Device, 2 = Boot Device
(SA) + 002Dh	00XXh	Erase Block Region 1 Information (refer to JEDEC JESD68-01 or JEP137 specifications) 00FFh, 0003h, 0000h, 0002h = 1 Gb 00FFh, 0001h, 0000h, 0002h = 512 Mb 00FFh, 0000h, 0000h, 0002h = 256 Mb 007Fh, 0000h, 0000h, 0002h = 128 Mb
(SA) + 002Eh	000Xh	
(SA) + 002Fh	0000h	
(SA) + 0030h	000Xh	
(SA) + 0031h	0000h	Erase Block Region 2 Information (refer to CFI publication 100)
(SA) + 0032h	0000h	
(SA) + 0033h	0000h	
(SA) + 0034h	0000h	
(SA) + 0035h	0000h	Erase Block Region 3 Information (refer to CFI publication 100)
(SA) + 0036h	0000h	
(SA) + 0037h	0000h	
(SA) + 0038h	0000h	
(SA) + 0039h	0000h	Erase Block Region 4 Information (refer to CFI publication 100)
(SA) + 003Ah	0000h	
(SA) + 003Bh	0000h	
(SA) + 003Ch	0000h	
(SA) + 003Dh	FFFFh	Reserved
(SA) + 003Eh	FFFFh	Reserved
(SA) + 003Fh	FFFFh	Reserved

Table 46 CFI primary vendor-specific extended query

Word address	Data	Description
(SA) + 0040h	0050h	Query-unique ASCII string “PRI”
(SA) + 0041h	0052h	
(SA) + 0042h	0049h	
(SA) + 0043h	0031h	Major version number, ASCII
(SA) + 0044h	0035h	Minor version number, ASCII
(SA) + 0045h	001Ch	Address Sensitive Unlock (Bits 1–0) 00b = Required 01b = Not required Process Technology (Bits 5–2) 0000b = 0.23 µm Floating Gate 0001b = 0.17 µm Floating Gate 0010b = 0.23 µm MIRRORBIT™ 0011b = 0.13 µm Floating Gate 0100b = 0.11 µm MIRRORBIT™ 0101b = 0.09 µm MIRRORBIT™ 0110b = 0.09 µm Floating Gate 0111b = 0.065 µm MIRRORBIT™ Eclipse 1000b = 0.065 µm MIRRORBIT™ 1001b = 0.045 µm MIRRORBIT™
(SA) + 0046h	0002h	Erase Suspend 0 = Not supported 1 = Read Only 2 = Read and Write
(SA) + 0047h	0001h	Sector Protect 00 = Not supported X = Number of sectors in smallest group
(SA) + 0048h	0000h	Temporary Sector Unprotect 00 = Not supported 01 = Supported
(SA) + 0049h	0008h	Sector Protect/Unprotect Scheme 04 = High Voltage method 05 = Software Command Locking method 08 = Advanced Sector Protection method
(SA) + 004Ah	0000h	Simultaneous Operation 00 = Not supported X = Number of banks
(SA) + 004Bh	0000h	Burst Mode type 00 = Not supported 01 = Supported
(SA) + 004Ch	0003h	Page Mode type 00 = Not supported 01 = 4 Word Page 02 = 8 Word Page 03 = 16 Word Page
(SA) + 004Dh	0000h	ACC (Acceleration) Supply Minimum 00 = Not supported D7–D4: Volt D3–D0: 100 mV

Table 46 CFI primary vendor-specific extended query (Continued)

Word address	Data	Description
(SA) + 004Eh	0000h	ACC (Acceleration) Supply Maximum 00 = Not Supported D7–D4: Volt D3–D0: 100 mV
(SA) + 004Fh	0004h (Bottom) 0005h (Top)	WP# Protection 00h = Flash device without WP Protect (No Boot) 01h = Eight 8 kB Sectors at TOP and Bottom with WP (Dual Boot) 02h = Bottom Boot Device with WP Protect (Bottom Boot) 03h = Top Boot Device with WP Protect (Top Boot) 04h = Uniform, Bottom WP Protect (Uniform Bottom Boot) 05h = Uniform, Top WP Protect (Uniform Top Boot) 06h = WP Protect for all sectors 07h = Uniform, Top and Bottom WP Protect
(SA) + 0050h	0001h	Program Suspend 00 = Not supported 01 = Supported
(SA) +0051h	0000h	Unlock Bypass 00 = Not supported 01 = Supported
(SA) + 0052h	0009h	Secured Silicon Sector (Customer OTP Area) Size 2^N (bytes)
(SA) + 0053h	008Fh	Software Features bit 0: status register polling (1 = supported, 0 = not supported) bit 1: DQ polling (1 = supported, 0 = not supported) bit 2: new program suspend/resume commands (1 = supported, 0 = not supported) bit 3: word programming (1 = supported, 0 = not supported) bit 4: bit-field programming (1 = supported, 0 = not supported) bit 5: autodetect programming (1 = supported, 0 = not supported) bit 6: RFU bit 7: multiple writes per Line (1 = supported, 0 = not supported)
(SA) + 0054h	0005h	Page Size = 2^N bytes
(SA) + 0055h	0006h	Erase Suspend Timeout Maximum < 2^N (µs)
(SA) + 0056h	0006h	Program Suspend Timeout Maximum < 2^N (µs)
(SA) + 0057h to (SA) + 0077h	FFFFh	Reserved
(SA) + 0078h	0006h	Embedded Hardware Reset Timeout Maximum < 2^N (µs) Reset with Reset Pin
(SA) + 0079h	0009h	Non-Embedded Hardware Reset Timeout Maximum < 2^N (µs) Power on Reset

7.3 Device ID and Common Flash Interface (ID-CFI) ASO Map

Table 47 Device ID and common flash interface (ID-CFI) ASO map

Word address	Data field	# of bytes	Data format	Example of actual data	Hex read out of example data
(SA) + 0080h	Size of Electronic Marking	1	Hex	19	0013h
(SA) + 0081h	Revision of Electronic Marking	1	Hex	1	0001h
(SA) + 0082h	Fab Lot #	7	Ascii	LD87270	004Ch, 0044h, 0038h, 0037h, 0032h, 0037h, 0030h
(SA) + 0089h	Wafer #	1	Hex	23	0017h
(SA) + 008Ah	Die X Coordinate	1	Hex	10	000Ah
(SA) + 008Bh	Die Y Coordinate	1	Hex	15	000Fh
(SA) + 008Ch	Class Lot#	7	Ascii	BR33150	0042h, 0052h, 0033h, 0033h, 0031h, 0035h, 0030h
(SA) + 0093h	Reserved for future	13	n/a	n/a	undefined
Fab Lot # + Wafer # + Die X Coordinate + Die Y Coordinate gives a unique ID for each device.					

8 Signal descriptions

8.1 Address and data configuration

Address and data are connected in parallel (ADP) via separate signal inputs and I/Os.

8.2 Input/Output summary

Table 48 I/O summary

Symbol	Type	Description
RESET#	Input	Hardware Reset. At V_{IL}, causes the device to reset control logic to its standby state, ready for reading array data.
CE#	Input	Chip Enable. At V_{IL}, selects the device for data transfer with the host memory controller.
OE#	Input	Output Enable. At V_{IL}, causes outputs to be actively driven. At V_{IH}, causes outputs to be high impedance (High-Z).
WE#	Input	Write Enable. At V_{IL}, indicates data transfer from host to device. At V_{IH}, indicates data transfer is from device to host.
A_{MAX}–A0	Input	Address inputs. A25–A0 for S29GL01GS A24–A0 for S29GL512S A23–A0 for S29GL256S A22–A0 for S29GL128S
DQ15–DQ0	Input/Output	Data inputs and outputs
WP#	Input	Write Protect. At V_{IL}, disables program and erase functions in the lowest or highest address 64-kword (128-kB) sector of the device. At V_{IH}, the sector is not protected. WP# has an internal pull up; When unconnected WP# is at V_{IH}.
RY/BY#	Output - open drain	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively engaged in an Embedded Algorithm such as erasing or programming. At High-Z, the device is ready for read or a new command write - requires external pull-up resistor to detect the High-Z state. Multiple devices may have their RY/BY# outputs tied together to detect when all devices are ready.
V_{CC}	Power Supply	Core power supply
V_{IO}	Power Supply	Versatile IO power supply.
V_{SS}	Power Supply	Power supplies ground
NC	No Connect	Not Connected internally. The pin/ball location may be used in printed circuit board (PCB) as part of a routing channel.
RFU	No Connect	Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.
DNU	Reserved	Do Not Use. Reserved for use by Infineon. The pin/ball is connected internally. The input has an internal pull down resistance to V_{SS}. The pin/ball can be left open or tied to V_{SS} on the PCB.

8.3 Versatile I/O feature

The maximum output voltage level driven by, and input levels acceptable to, the device are determined by the V_{IO} power supply. This supply allows the device to drive and receive signals to and from other devices on the same bus having interface signal levels different from the device core voltage.

8.4 Ready/Busy# (RY/BY#)

RY/BY# is a dedicated, open drain output pin that indicates whether an Embedded Algorithm, Power-On Reset (POR), or Hardware Reset is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in a command sequence, when V_{CC} is above V_{CC} minimum during POR, or after the falling edge of RESET#. Since RY/BY# is an open drain output, several RY/BY# pins can be tied together in parallel with a pull up resistor to V_{IO}.

If the output is Low (Busy), the device is actively erasing, programming, or resetting. (This includes programming in the Erase Suspend mode). If the output is High (Ready), the device is ready to read data (including during the Erase Suspend mode), or is in the standby mode.

Table 15 shows the outputs for RY/BY# in each operation.

If an Embedded algorithm has failed (Program / Erase failure as result of max pulses or Sector is locked), RY/BY# will stay LOW (busy) until status register bits 4 and 5 are cleared and the reset command is issued. This includes Erase or Programming on a locked sector.

8.5 Hardware Reset

The RESET# input provides a hardware method of resetting the device to standby state. When RESET# is driven LOW for at least a period of t_{RP}, the device immediately:

- terminates any operation in progress,
- exits any ASO,
- tristates all outputs,
- resets the status register,
- resets the EAC to standby state.
- CE# is ignored for the duration of the reset operation (t_{RPH}).
- To meet the Reset current specification (I_{CC5}) CE# must be held HIGH.

To ensure data integrity any operation that was interrupted should be reinitiated once the device is ready to accept another command sequence.

9 Signal protocols

The following sections describe the host system interface signal behavior and timing for the 29GL-S family flash devices.

9.1 Interface states

Table 49 describes the required value of each interface signal for each interface state.

Table 49 Interface states

Interface state	V_{CC}	V_{IO}	RESET#	CE#	OE#	WE#	A_{MAX}–A0	DQ15–DQ0
Power-Off with Hardware Data Protection	$< V_{LKO}$	$\leq V_{CC}$	X	X	X	X	X	High-Z
Power-On (Cold) Reset	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	X	X	X	X	X	High-Z
Hardware (Warm) Reset	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	L	X	X	X	X	High-Z
Interface Standby	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	H	H	X	X	X	High-Z
Automatic Sleep[70, 71]	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	H	L	X	X	Valid	Output available
Read with Output Disable[72]	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	H	L	H	H	Valid	High-Z
Random Read	$\geq V_{CC}$ min	$\geq V_{IO}$ min	H	L	L	H	Valid	Output valid
Page Read	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	H	L	L	H	A_{MAX}–A4 valid A3–A0 modified	Output valid
Write	$\geq V_{CC}$ min	$\geq V_{IO}$ min $\leq V_{CC}$	H	L	H	L	Valid	Input valid

Legend:
L = V_{IL}
H = V_{IH}
X = either V_{IL} or V_{IH}
L/H = rising edge
H/L = falling edge
Valid = all bus signals have stable L or H level
Modified = valid state different from a previous valid state
Available = read data is internally stored with output driver controlled by OE#

Notes
70. WE# and OE# can not be at V_{IL} at the same time.
71. Automatic Sleep is a read/write operation where data has been driven on the bus for an extended period, without CE# going HIGH and the device internal logic has gone into standby mode to conserve power.
72. Read with Output Disable is a read initiated with OE# HIGH.

9.2 Power-Off with Hardware Data Protection

The memory is considered to be powered off when the core power supply (V_{CC}) drops below the lock-out voltage (V_{LKO}). When V_{CC} is below V_{LKO}, the entire memory array is protected against a program or erase operation. This ensures that no spurious alteration of the memory content can occur during power transition. During a power supply transition down to Power-Off, V_{IO} should remain less than or equal to V_{CC}.

If V_{CC} goes below V_{RST} (Min) then returns above V_{RST} (Min) to V_{CC} minimum, the Power-On Reset interface state is entered and the EAC starts the Cold Reset Embedded Algorithm.

9.3 Power Conservation Modes

9.3.1 Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CE# = HIGH). All inputs are ignored in this state and all outputs except RY/BY# are high impedance. RY/BY# is a direct output of the EAC, not controlled by the Host Interface.

9.3.2 Automatic Sleep

The automatic sleep mode reduces device interface energy consumption to the sleep level (I_{CC6}) following the completion of a random read access time. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. While in sleep mode, output data is latched and always available to the system. Output of the data depends on the level of the OE# signal but, the automatic sleep mode current is independent of the OE# signal level. Standard address access timings (t_{ACC} or t_{PACC}) provide new data when addresses are changed. I_{CC6} in **"DC characteristics"** on page 78 represents the automatic sleep mode current specification.

Automatic sleep helps reduce current consumption especially when the host system clock is slowed for power reduction. During slow system clock periods, read and write cycles may extend many times their length versus when the system is operating at high speed. Even though CE# may be LOW throughout these extended data transfer cycles, the memory device host interface will go to the Automatic Sleep current at t_{ACC} + 30 ns. The device will remain at the Automatic Sleep current for t_{ASSB}. Then the device will transition to the standby current level. This keeps the memory at the Automatic Sleep or standby power level for most of the long duration data transfer cycles, rather than consuming full read power all the time that the memory device is selected by the host system.

However, the EAC operates independent of the automatic sleep mode of the host interface and will continue to draw current during an active Embedded Algorithm. Only when both the host interface and EAC are in their standby states is the standby level current achieved.

9.4 Read

9.4.1 Read with Output Disable

When the CE# signal is asserted LOW, the host system memory controller begins a read or write data transfer. Often there is a period at the beginning of a data transfer when CE# is LOW, address is valid, OE# is HIGH, and WE# is HIGH. During this state a read access is assumed and the Random Read process is started while the data outputs remain at high impedance. If the OE# signal goes LOW, the interface transitions to the Random Read state, with data outputs actively driven. If the WE# signal is asserted LOW, the interface transitions to the Write state. Note, OE# and WE# should never be LOW at the same time to ensure no data bus contention between the host system and memory.

9.4.2 Random (Asynchronous) Read

When the host system interface selects the memory device by driving CE# LOW, the device interface leaves the Standby state. If WE# is HIGH when CE# goes LOW, a random read access is started. The data output depends on the address map mode and the address provided at the time the read access is started.

The data appears on DQ15–DQ0 when CE# is LOW, OE# is LOW, WE# remains HIGH, address remains stable, and the asynchronous access times are satisfied. Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable CE# to valid data at the outputs. In order for the read data to be driven on to the data outputs the OE# signal must be LOW at least the output enable time (t_{OE}) before valid data is available.

At the completion of the random access time from CE# active (t_{CE}), address stable (t_{ACC}), or OE# active (t_{OE}), whichever occurs latest, the data outputs will provide valid read data from the currently active address map mode. If CE# remains LOW and any of the A_{MAX} to A4 address signals change to a new value, a new random read access begins. If CE# remains LOW and OE# goes HIGH the interface transitions to the Read with Output Disable state. If CE# remains LOW, OE# goes HIGH, and WE# goes LOW, the interface transitions to the Write state. If CE# returns HIGH, the interface goes to the Standby state. Back to Back accesses, in which CE# remains LOW between accesses, requires an address change to initiate the second access. See **“Asynchronous Read operations”** on page 85.

9.4.3 Page Read

After a Random Read access is completed, if CE# remains LOW, OE# remains LOW, the A_{MAX} to A4 address signals remain stable, and any of the A3 to A0 address signals change, a new access within the same page begins. The Page Read completes much faster (t_{PACC}) than a Random Read access.

9.5 Write

9.5.1 Asynchronous Write

When WE# goes Low after CE is LOW, there is a transition from one of the read states to the Write state. If WE# is LOW before CE# goes LOW, there is a transition from the Standby state directly to the Write state without beginning a read access.

When CE# is LOW, OE# is HIGH, and WE# goes LOW, a write data transfer begins. Note, OE# and WE# should never be LOW at the same time to ensure no data bus contention between the host system and memory. When the asynchronous write cycle timing requirements are met the WE# can go HIGH to capture the address and data values in to EAC command memory.

Address is captured by the falling edge of WE# or CE#, whichever occurs later. Data is captured by the rising edge of WE# or CE#, whichever occurs earlier.

When CE# is LOW before WE# goes LOW and stays LOW after WE# goes HIGH, the access is called a WE# controlled Write. When WE# is HIGH and CE# goes HIGH, there is a transition to the Standby state. If CE# remains LOW and WE# goes HIGH, there is a transition to the Read with Output Disable state.

When WE# is LOW before CE# goes LOW and remains LOW after CE# goes HIGH, the access is called a CE# controlled Write. A CE# controlled Write transitions to the Standby state.

If WE# is LOW before CE# goes LOW, the write transfer is started by CE# going LOW. If WE# is LOW after CE# goes HIGH, the address and data are captured by the rising edge of CE#. These cases are referred to as CE# controlled write state transitions.

Write followed by Read accesses, in which CE# remains LOW between accesses, requires an address change to initiate the following read access.

Back to Back accesses, in which CE# remains LOW between accesses, requires an address change to initiate the second access.

The EAC command memory array is not readable by the host system and has no ASO. The EAC examines the address and data in each write transfer to determine if the write is part of a legal command sequence. When a legal command sequence is complete the EAC will initiate the appropriate EA.

9.5.2 Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on WE# will not initiate a write cycle.

9.5.3 Logical Inhibit

Write cycles are inhibited by holding OE# at V_{IL}, or CE# at V_{IH}, or WE# at V_{IH}. To initiate a write cycle, CE# and WE# must be LOW (V_{IL}) while OE# is HIGH (V_{IH}).

10 Electrical specifications

10.1 Absolute maximum ratings

Table 50 Absolute maximum ratings

Storage temperature plastic packages	–65°C to +150°C
Ambient temperature with power applied	–65°C to +125°C
Voltage with respect to ground	
All pins other than RESET# [73]	–0.5 V to (V_{IO} + 0.5 V)
RESET#[73]	–0.5 V to (V_{CC} + 0.5 V)
Output short circuit current[74]	100 mA
V_{CC}	–0.5 V to +4.0 V
V_{IO}	–0.5 V to +4.0 V

10.2 Latchup characteristics

This product complies with JEDEC standard JESD78C latchup testing requirements.

10.3 Thermal resistance

Table 51 Thermal resistance

Parameter	Description	Part number	LAA064	LAE064	TS056	VBU056	Unit
Theta JA	Thermal resistance (junction to ambient)	S29GL01GS	19.8	27.3	38	–	°C/W
		S29GL512S	22.2	30.4	44	30.2	
		S29GL256S	24.1	33	46	34.47	
		S29GL128S	25.2	34.1	56.7	35.94	
Theta JB	Thermal resistance (junction to board)	S29GL01GS	6.5	5.7	30	–	
		S29GL512S	10.5	8.4	41	8.14	
		S29GL256S	11.7	12.2	54.7	12.1	
		S29GL128S	13	13.70	60	13.64	
Theta JC	Thermal resistance (junction to case)	S29GL01GS	5.19	6.0	11.2	–	
		S29GL512S	6.8	7.5	15	8	
		S29GL256S	7.4	10.1	18	10.11	
		S29GL128S	10.3	9.74	18	11.36	

Notes

73. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See **Figure 11**. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See **Figure 12**.
74. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
75. Stresses above those listed under **Absolute maximum ratings** may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

10.4 Operating ranges

10.4.1 Temperature ranges

Table 52 Temperature ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient temperature	T_A	Industrial (I)	–40	+85	°C
		Industrial plus (V)	–40	+105	
		Automotive, AEC-Q100 grade 3 (A)	–40	+85	
		Automotive, AEC-Q100 grade 2 (B)	–40	+105	

10.4.2 Power supply voltages

Table 53 Power supply voltages

V_{CC}	2.7 V to 3.6 V
V_{IO}	1.65 V to V_{CC} + 200 mV

Operating ranges define those limits between which the functionality of the device is guaranteed.

10.4.3 Power-up and power-down

During power-up or power-down V_{CC} must always be greater than or equal to V_{IO} ($V_{CC} \geq V_{IO}$).

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and V_{IO} both rise above, and stay above, the minimum V_{CC} and V_{IO} thresholds. During t_{VCS} the device is performing power on reset operations.

During power-down or voltage drops below V_{CC} Lockout maximum (V_{LKO}), the V_{CC} and V_{IO} voltages must drop below V_{CC} Reset (V_{RST}) minimum for a period of t_{PD} for the part to initialize correctly when V_{CC} and V_{IO} again rise to their operating ranges. See **Figure 10**. If during a voltage drop the V_{CC} stays above V_{LKO} maximum the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If the part locks up from improper initialization, a hardware reset can be used to initialize the part correctly.

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 µF). At no time should V_{IO} be greater then 200 mV above V_{CC} ($V_{CC} \geq V_{IO}$ – 200 mV).

Table 54 Power-up/power-down voltage and timing

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} power supply	2.7	3.6	V
V_{LKO}	V_{CC} level below which re-initialization is required[76]	2.25	2.5	V
V_{RST}	V_{CC} and V_{IO} Low voltage needed to ensure initialization will occur[76]	1.0	–	V
t_{VCS}	V_{CC} and $V_{IO} \geq$ minimum to first access[76]	300	–	µs
t_{PD}	Duration of $V_{CC} \leq V_{RST}$(min)[76]	15	–	µs

Note
76.Not 100% tested.

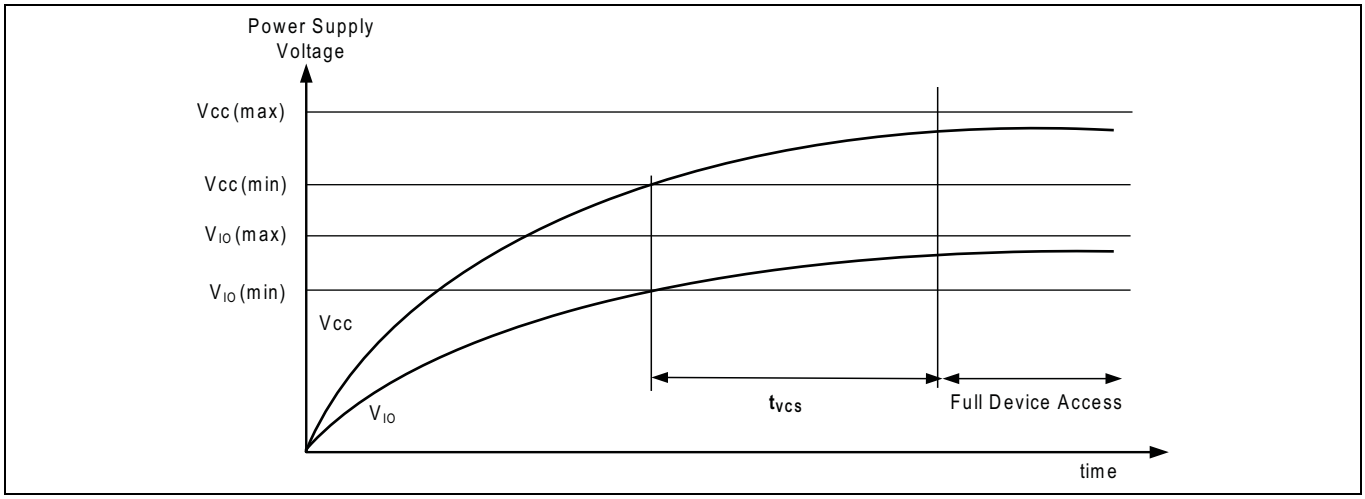


Figure 9 Power-up

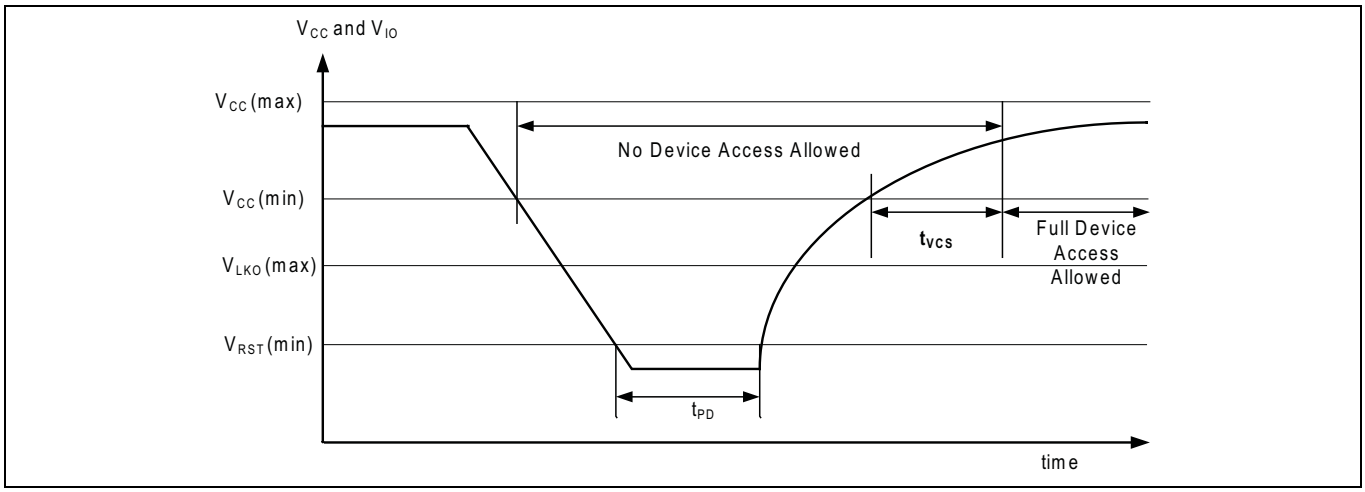


Figure 10 Power-down and voltage drop

10.4.4 Input signal overshoot

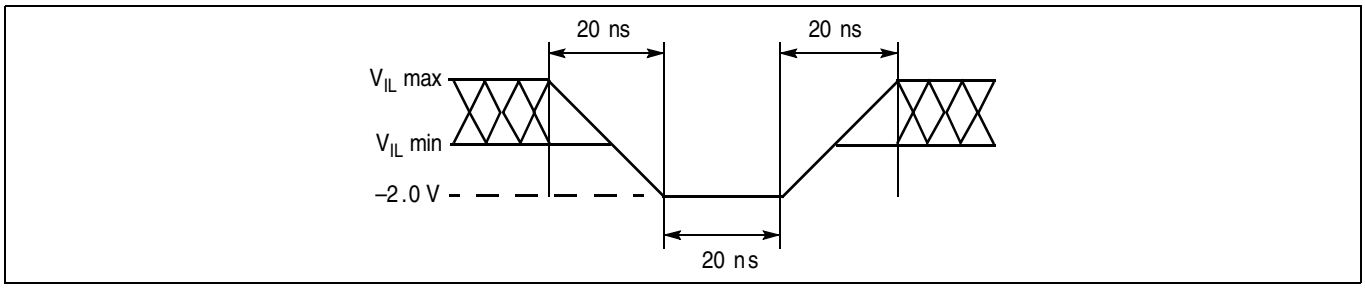


Figure 11 Maximum negative overshoot waveform

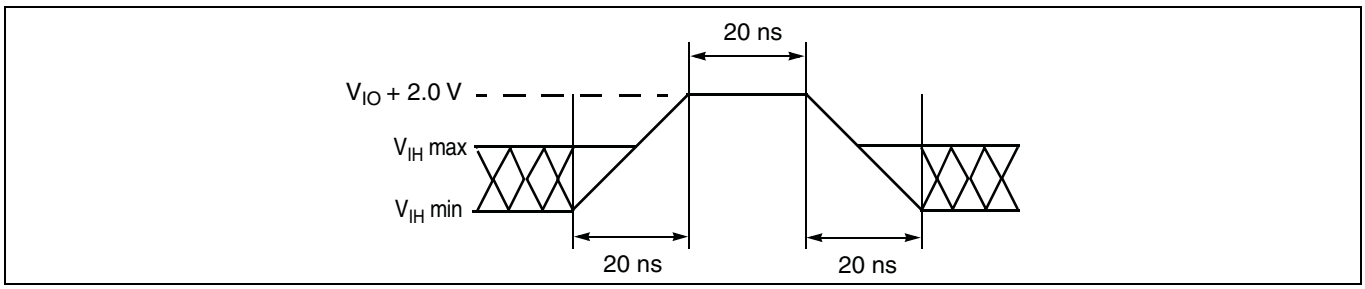


Figure 12 Maximum positive overshoot waveform

10.5 DC characteristics

Table 55 DC characteristics (–40°C to +85°C)

Parameter	Description	Test conditions	Min	Typ[77]	Max	Unit
I_{LI}	Input load current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	+0.02	±1.0	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	+0.02	±1.0	µA
I_{CC1}	V_{CC} active read current	CE# = V_{IL}, OE# = V_{IH}, address switching @ 5 MHz, $V_{CC} = V_{CC}$ max	–	55	60	mA
I_{CC2}	V_{CC} intra-page read current	CE# = V_{IL}, OE# = V_{IH}, address switching @ 33 MHz, $V_{CC} = V_{CC}$ max	–	9	25	mA
I_{CC3}	V_{CC} active erase/program current[77, 78]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ max	–	45	100	mA
I_{CC4}	V_{CC} standby current	CE#, RESET#, OE# = V_{IH}, $V_{IH} = V_{IO}$. $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max	–	70	100	µA
I_{CC5}	V_{CC} reset current[77, 79]	CE# = V_{IH}, RESET# = V_{IL}, $V_{CC} = V_{CC}$ max	–	10	20	mA
I_{CC6}	Automatic sleep mode[80]	$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ACC} + 30 ns	–	3	6	mA
		$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ASSB}	–	100	150	µA
I_{CC7}	V_{CC} current during power up[77, 81]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, $V_{CC} = V_{CC}$ max,	–	53	80	mA
V_{IL}	Input low voltage[82]		–0.5	–	0.3 × V_{IO}	V
V_{IH}	Input high voltage[82]		0.7 × V_{IO}	–	V_{IO} + 0.4	V
V_{OL}	Output low voltage[82, 84]	I_{OL} = 100 µA for DQ15–DQ0; I_{OL} = 2 mA for RY/BY#	–	–	0.15 × V_{IO}	V
V_{OH}	Output high voltage[82]	I_{OH} = 100 µA	0.85 × V_{IO}	–	–	V
V_{LKO}	Low V_{CC} lock-out voltage[77]		2.25	–	2.5	V
V_{RST}	Low V_{CC} power on reset voltage[77]		–	1.0	–	V

Notes

77. Not 100% tested.
78. I_{CC} active while Embedded Algorithm is in progress.
79. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC5} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
80. Automatic sleep mode enables the lower power mode when addresses remain stable for the specified designated time.
81. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
82. V_{IO} = 1.65 V to V_{CC} or 2.7 V to V_{CC} depending on the model.
83. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/O pins cannot operate at >1.8 V.
84. The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.

Table 56 DC characteristics (–40°C to +105°C)

Parameter	Description	Test conditions	Min	Typ[85]	Max	Unit
I_{LI}	Input load current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	+0.02	±1.0	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	+0.02	±1.0	µA
I_{CC1}	V_{CC} active read current	CE# = V_{IL}, OE# = V_{IH}, address switching @ 5 MHz, $V_{CC} = V_{CC}$ max	–	55	60	mA
I_{CC2}	V_{CC} intra-page read current	CE# = V_{IL}, OE# = V_{IH}, address switching @ 33 MHz, $V_{CC} = V_{CC}$ max	–	9	25	mA
I_{CC3}	V_{CC} active erase/program current[85, 86]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ max	–	45	100	mA
I_{CC4}	V_{CC} standby current	CE#, RESET#, OE# = V_{IH}, $V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max	–	70	200	µA
I_{CC5}	V_{CC} reset current[85, 87]	CE# = V_{IH}, RESET# = V_{IL}, $V_{CC} = V_{CC}$ max	–	10	20	mA
I_{CC6}	Automatic sleep mode[88]	$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ACC} + 30 ns	–	3	6	mA
		$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ASSB}	–	100	200	µA
I_{CC7}	V_{CC} current during power-up[85, 89]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, $V_{CC} = V_{CC}$ max	–	53	80	mA
V_{IL}	Input low voltage[90]		–0.5	–	0.3 × V_{IO}	V
V_{IH}	Input high voltage[90]		0.7 × V_{IO}	–	V_{IO} + 0.4	V
V_{OL}	Output low voltage[90, 92]	I_{OL} = 100 µA for DQ15–DQ0; I_{OL} = 2 mA for RY/BY#	–	–	0.15 × V_{IO}	V
V_{OH}	Output high voltage[90]	I_{OH} = 100 µA	0.85 × V_{IO}	–	–	V
V_{LKO}	Low V_{CC} lock-out voltage[85]		2.25	–	2.5	V
V_{RST}	Low V_{CC} power on reset voltage[85]		–	1.0	–	V

Notes

85. Not 100% tested.
86. I_{CC} active while embedded algorithm is in progress.
87. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
88. Automatic sleep mode enables the lower power mode when addresses remain stable for the specified designated time.
89. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
90. V_{IO} = 1.65 V to V_{CC} or 2.7 V to V_{CC} depending on the model.
91. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/O pins cannot operate at >1.8 V.
92. The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.

10.6 Capacitance characteristics

Table 57 Connector capacitance for FBGA (LAA) package

Parameter symbol	Parameter description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	8	9	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	5	7	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	4	8	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	4	pF

Table 58 Connector capacitance for FBGA (LAE) package

Parameter symbol	Parameter description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	7	8	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	5	6	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	3	7	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	4	pF

Table 59 Connector capacitance for TSOP package

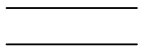
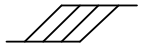
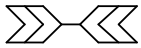
Parameter symbol	Parameter description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	7	8	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	5	6	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	3	7	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	4	pF

Notes
93. Sampled, not 100% tested.
94. Test conditions $T_A = 25°C$, f = 1.0 MHz.
95. Sampled, not 100% tested.
96. Test conditions $T_A = 25°C$, f = 1.0 MHz.
97. Sampled, not 100% tested.
98. Test conditions $T_A = 25°C$, f = 1.0 MHz.

11 Timing specifications

11.1 Key to switching waveforms

Table 60 Key to switching waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't care, any change permitted	Changing, state unknown
	Does not apply	Center line is high impedance state (High-Z)

11.2 AC test conditions

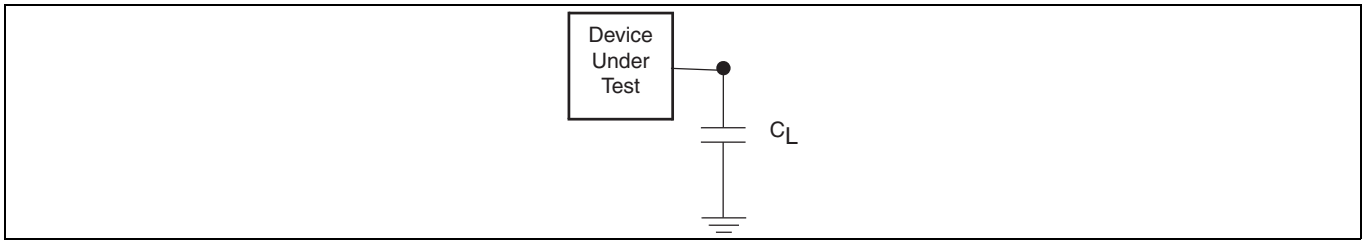


Figure 13 Test setup

Table 61 Test specification

Parameter	All speeds	Units
Output load capacitance, C_L	30	pF
Input rise and fall times[99]	1.5	ns
Input pulse levels	0.0–V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

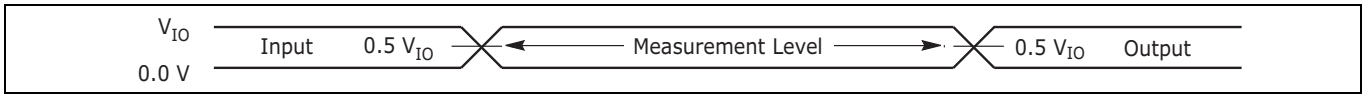


Figure 14 Input waveforms and measurement levels

Note
99.Measured between V_{IL} max and V_{IH} min.

11.3 Power-on reset (POR) and warm reset

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 µF).

Table 62 Power ON and Reset parameters

Parameter	Description	Limit	Value	Unit
t_{VCS}	V_{CC} Setup Time to first access[100, 101]	Min	300	µs
t_{VIOS}	V_{IO} Setup Time to first access[100, 101]	Min	300	µs
t_{RPH}	RESET# LOW to CE# LOW	Min	35	µs
t_{RP}	RESET# Pulse Width	Min	200	ns
t_{RH}	Time between RESET# (HIGH) and CE# (LOW)	Min	50	ns
t_{CEH}	CE# Pulse Width High	Min	20	ns

Notes

100. Not 100% tested.
101. Timing measured from V_{CC} reaching V_{CC} minimum and V_{IO} reaching V_{IO} minimum to V_{IH} on Reset and V_{IL} on CE#.
102. RESET# Low is optional during POR. If RESET is asserted during POR, the later of t_{RPH}, t_{VIOS}, or t_{VCS} will determine when CE# may go LOW. If RESET# remains LOW after t_{VIOS}, or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIOS}, or t_{VCS}. RESET must also be HIGH t_{RH} before CE# goes LOW.
103. $V_{CC} \geq V_{IO}$ - 200 mV during power-up.
104. V_{CC} and V_{IO} ramp rate can be non-linear.
105. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

11.3.1 Power-on (Cold) Reset (POR)

During the rise of power supplies the V_{IO} supply voltage must remain less than or equal to the V_{CC} supply voltage. V_{IH} also must remain less than or equal to the V_{IO} supply.

The Cold Reset Embedded Algorithm requires a relatively long, hundreds of µs, period (t_{VCS}) to load all of the EAC algorithms and default state from non-volatile memory. During the Cold Reset period all control signals including CE# and RESET# are ignored. If CE# is LOW during t_{VCS} the device may draw higher than normal POR current during t_{VCS} but the level of CE# will not affect the Cold Reset EA. CE# or OE# must transition from HIGH to LOW after t_{VCS} for a valid read or write operation. RESET# may be HIGH or LOW during t_{VCS}. If RESET# is LOW during t_{VCS} it may remain LOW at the end of t_{VCS} to hold the device in the Hardware Reset state. If RESET# is HIGH at the end of t_{VCS} the device will go to the Standby state.

When power is first applied, with supply voltage below V_{RST} then rising to reach operating range minimum, internal device configuration and warm reset activities are initiated. CE# is ignored for the duration of the POR operation (t_{VCS} or t_{VIOS}). RESET# LOW during this POR period is optional. If RESET# is driven LOW during POR it must satisfy the Hardware Reset parameters t_{RP} and t_{RPH}. In which case the Reset operations will be completed at the later of t_{VCS} or t_{VIOS} or t_{RPH}.

During Cold Reset the device will draw I_{CC7} current.

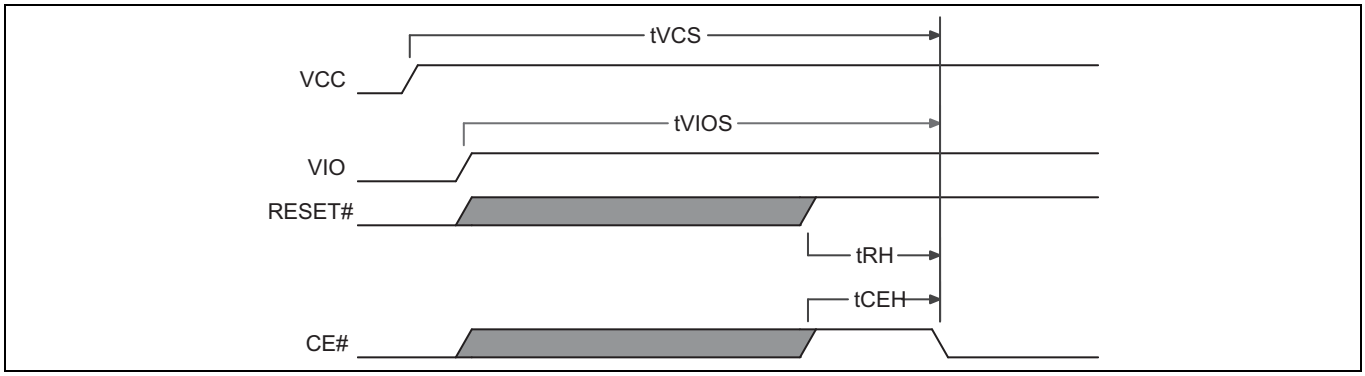


Figure 15 Power-up diagram

11.3.2 Hardware (Warm) Reset

During Hardware Reset (t_{RPH}) the device will draw I_{CC5} current.

When RESET# continues to be held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater.

If a Cold Reset has not been completed by the device when RESET# is asserted LOW after t_{VCS}, the Cold Reset# EA will be performed instead of the Warm RESET#, requiring t_{VCS} time to complete.

See **Figure 16**.

After the device has completed POR and entered the Standby state, any later transition to the Hardware Reset state will initiate the Warm Reset Embedded Algorithm. A Warm Reset is much shorter than a Cold Reset, taking tens of µs (t_{RPH}) to complete. During the Warm Reset EA, any in progress Embedded Algorithm is stopped and the EAC is returned to its POR state without reloading EAC algorithms from non-volatile memory. After the Warm Reset EA completes, the interface will remain in the Hardware Reset state if RESET# remains LOW. When RESET# returns HIGH the interface will transit to the Standby state. If RESET# is HIGH at the end of the Warm Reset EA, the interface will directly transit to the Standby state.

If POR has not been properly completed by the end of t_{VCS}, a later transition to the Hardware Reset state will cause a transition to the Power-on Reset interface state and initiate the Cold Reset Embedded Algorithm. This ensures the device can complete a Cold Reset even if some aspect of the system Power-On voltage ramp-up causes the POR to not initiate or complete correctly. The RY/BY# pin is LOW during cold or warm reset as an indication that the device is busy performing reset operations.

Hardware Reset is initiated by the RESET# signal going to V_{IL}.

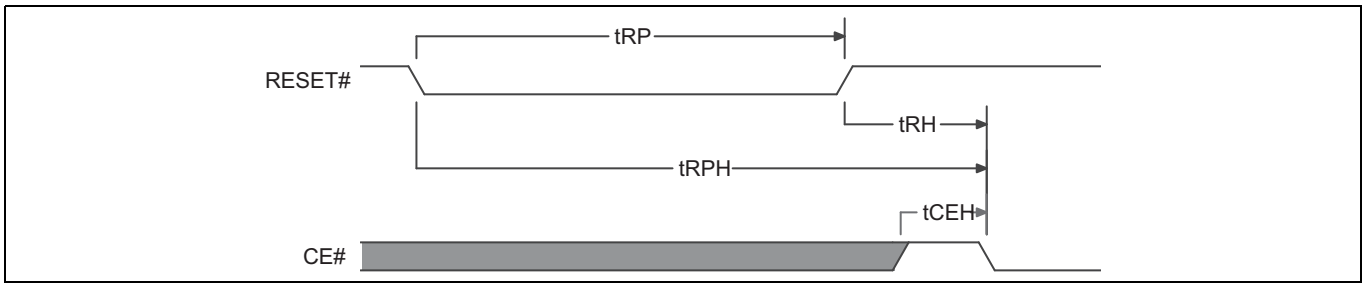


Figure 16 Hardware Reset

11.4 AC characteristics

11.4.1 Asynchronous Read operations

Table 63 Read Operation $V_{IO} = V_{CC}$ = 2.7 V to 3.6 V (–40°C to +85°C)

Parameter		Description		Test setup		Speed option			Unit
JEDEC	Std					90	100	110	
t_{AVAV}	t_{RC}	Read Cycle Time[106]		128 Mb, 256 Mb	Min	90	100	–	ns
				512 Mb, 1 Gb		–	100	110	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	128 Mb, 256 Mb	Max	90	100	–	ns
				512 Mb, 1 Gb		–	100	110	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	128 Mb, 256 Mb	Max	90	100	–	ns
				512 Mb, 1 Gb		–	100	110	
	t_{PACC}	Page Access Time		128 Mb, 256 Mb	Max	15	20	–	ns
				512 Mb, 1 Gb		–	15	20	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25			ns
t_{AXQX}	t_{OH}	Output Hold time from addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
t_{EHQZ}	t_{DF}	Chip Enable or Output Enable to Output High-Z[106]			Max	15			ns
	t_{OEH}	Output Enable Hold Time[106]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{ASSB}	Automatic Sleep to Standby time[106]		CE# = V_{IL}, address stable	Typ	5			µs
					Max	8			µs

Note
106.Not 100% tested.

Table 64 Read Operation V_{IO} = 1.65 V to V_{CC}, V_{CC} = 2.7 V to 3.6 V (–40°C to +85°C)

Parameter		Description		Test setup		Speed options			Unit
JEDEC	Std					100	110	120	
t_{AVAV}	t_{RC}	Read Cycle time[107]		128 Mb, 256 Mb	Min	100	110	–	ns
				512 Mb, 1 Gb		–	110	120	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	128 Mb, 256 Mb	Max	100	110	–	ns
				512 Mb, 1 Gb		–	110	120	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	128 Mb, 256 Mb	Max	100	110	–	ns
				512 Mb, 1 Gb		–	110	120	
	t_{PACC}	Page Access time		128 Mb, 256 Mb	Max	25	30	–	ns
				512 Mb, 1 Gb		–	25	30	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35			ns
t_{AXQX}	t_{OH}	Output Hold time from addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
t_{EHQZ}	t_{DF}	Chip Enable or Output Enable to Output High-Z[107]			Max	20			ns
	t_{OEH}	Output Enable Hold Time[107]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{ASSB}	Automatic Sleep to Standby time[107]		CE# = V_{IL}, address stable	Typ	5			µs
					Max	8			µs

Note
107.Not 100% tested.

Table 65 Read Operation $V_{IO} = V_{CC}$ = 2.7 V to 3.6 V (–40°C to +105°C)

Parameter		Description		Test Setup		Speed Option			Unit
JEDEC	Std					100	110	120	
t_{AVAV}	t_{RC}	Read Cycle time[108]		128 Mb, 256 Mb	Min	100	110	–	ns
				512 Mb, 1 Gb		–	110	120	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	128 Mb, 256 Mb	Max	100	110	–	ns
				512 Mb, 1 Gb		–	110	120	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	128 Mb, 256 Mb	Max	100	110	–	ns
				512 Mb, 1 Gb		–	110	120	
	t_{PACC}	Page Access time		128 Mb, 256 Mb	Max	15	20	–	ns
				512 Mb, 1 Gb		–	15	20	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25			ns
t_{AXQX}	t_{OH}	Output Hold time from addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
t_{EHQZ}	t_{DF}	Chip Enable or Output Enable to Output High-Z[108]			Max	15			ns
	t_{OEH}	Output Enable Hold time[108]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{ASSB}	Automatic Sleep to Standby time[108]		CE# = V_{IL}, address stable	Typ	5			µs
					Max	8			µs

Note
108.Not 100% tested.

Table 66 Read Operation V_{IO} = 1.65 V to V_{CC}, V_{CC} = 2.7 V to 3.6 V (–40°C to +105°C)

Parameter		Description		Test Setup		Speed Option			Unit
JEDEC	Std					110	120	130	
t_{AVAV}	t_{RC}	Read Cycle time[109]		128 Mb, 256 Mb	Min	110	120	–	ns
				512 Mb, 1 Gb		–	120	130	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	128 Mb, 256 Mb	Max	110	120	–	ns
				512 Mb, 1 Gb		–	120	130	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	128 Mb, 256 Mb	Max	110	120	–	ns
				512 Mb, 1 Gb		–	120	130	
	t_{PACC}	Page Access time		128 Mb, 256 Mb	Max	25	30	–	ns
				512 Mb, 1 Gb		–	25	30	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35			ns
t_{AXQX}	t_{OH}	Output Hold time from addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
t_{EHQZ}	t_{DF}	Chip Enable or Output Enable to Output High-Z[109]			Max	20			ns
	t_{OEH}	Output Enable Hold time[109]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{ASSB}	Automatic Sleep to Standby time [109]		CE# = V_{IL}, address stable	Typ	5			µs
					Max	8			µs

Note
109.Not 100% tested.

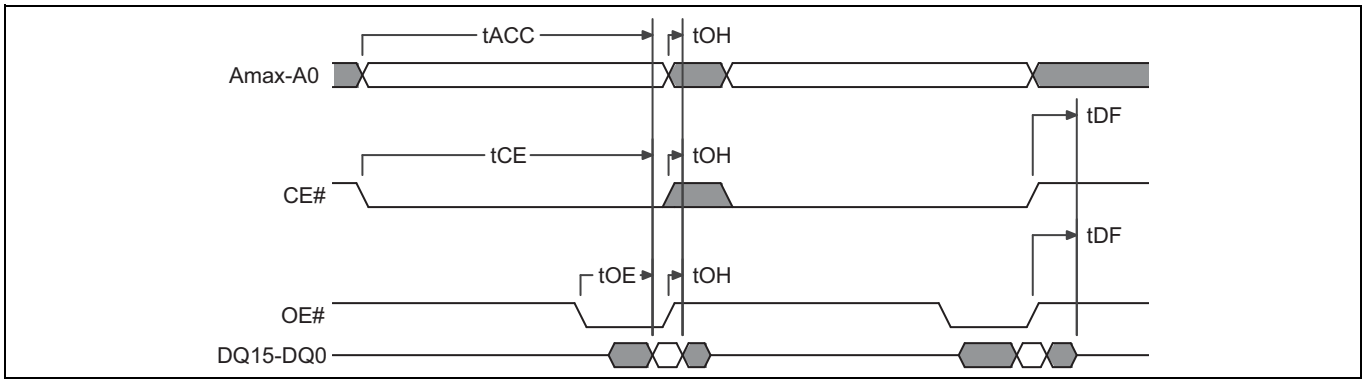


Figure 17 Back to Back Read (t_{ACC}) Operation timing diagram

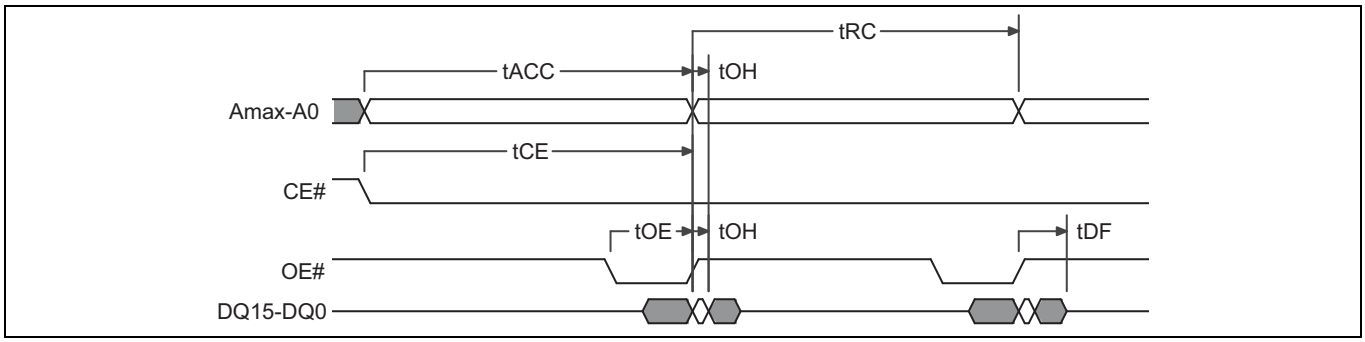


Figure 18 Back to Back Read Operation (t_{RC}) timing diagram

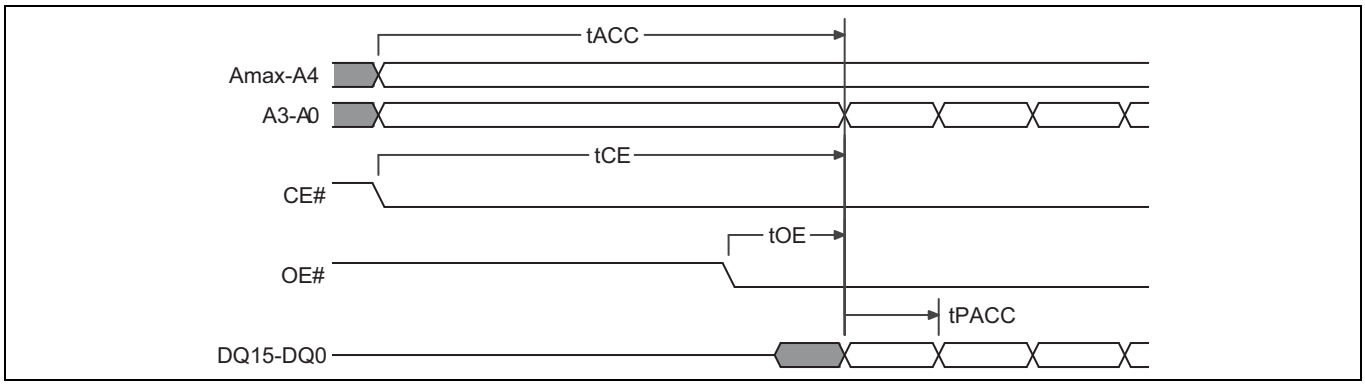


Figure 19 Page Read timing diagram

Notes

110. Back to Back operations, in which CE# remains Low between accesses, requires an address change to initiate the second access.
111. Word Configuration: Toggle A0, A1, A2, and A3.

11.4.2 Asynchronous Write Operations

Table 67 Write Operations

Parameter		Description		V_{IO} = 2.7 V to V_{CC}	V_{IO} = 1.65 V to V_{CC}	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle time[112]	Min	60		ns
t_{AVWL}	t_{AS}	Address Setup time	Min	0		ns
	t_{ASO}	Address setup time to OE# LOW during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold time	Min	45		ns
	t_{AHT}	Address Hold time From CE# or OE# HIGH during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup time	Min	30		ns
t_{WHDX}	t_{DH}	Data Hold time	Min	0		ns
	t_{OEPH}	Output Enable HIGH during toggle bit polling or following status register read.	Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery time Before Write (OE# HIGH to WE# LOW)	Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup time	Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold time	Min	0		ns
t_{WLWH}	t_{WP}	WE# Pulse Width	Min	25		ns
t_{WHWL}	t_{WPH}	WE# Pulse Width HIGH	Min	20		ns

Note
112.Not 100% tested.

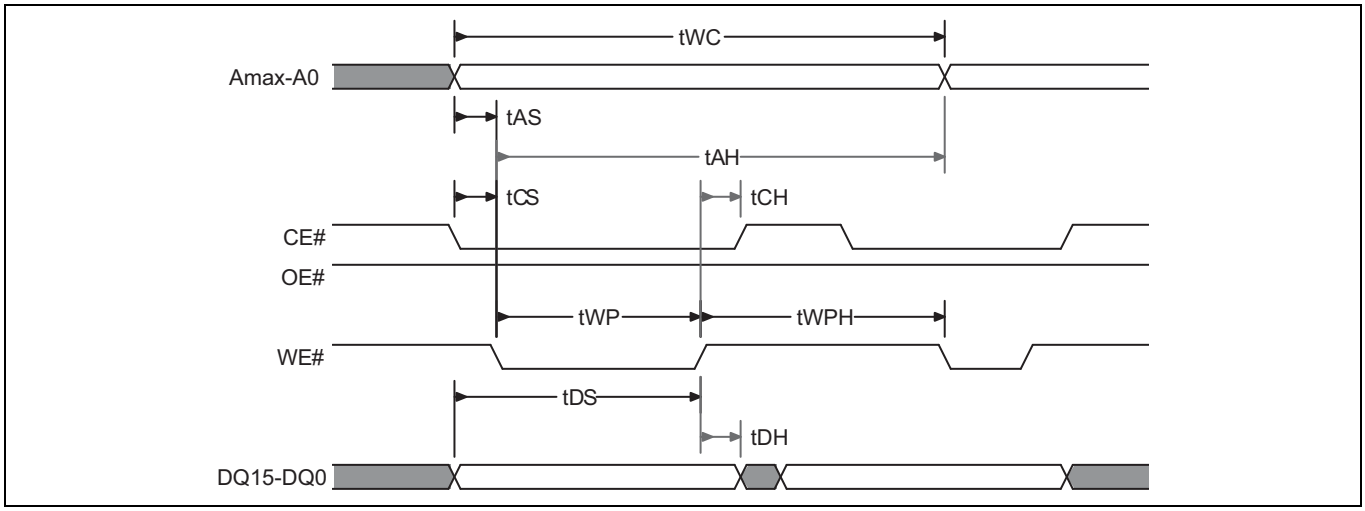


Figure 20 Back to Back Write Operation timing diagram

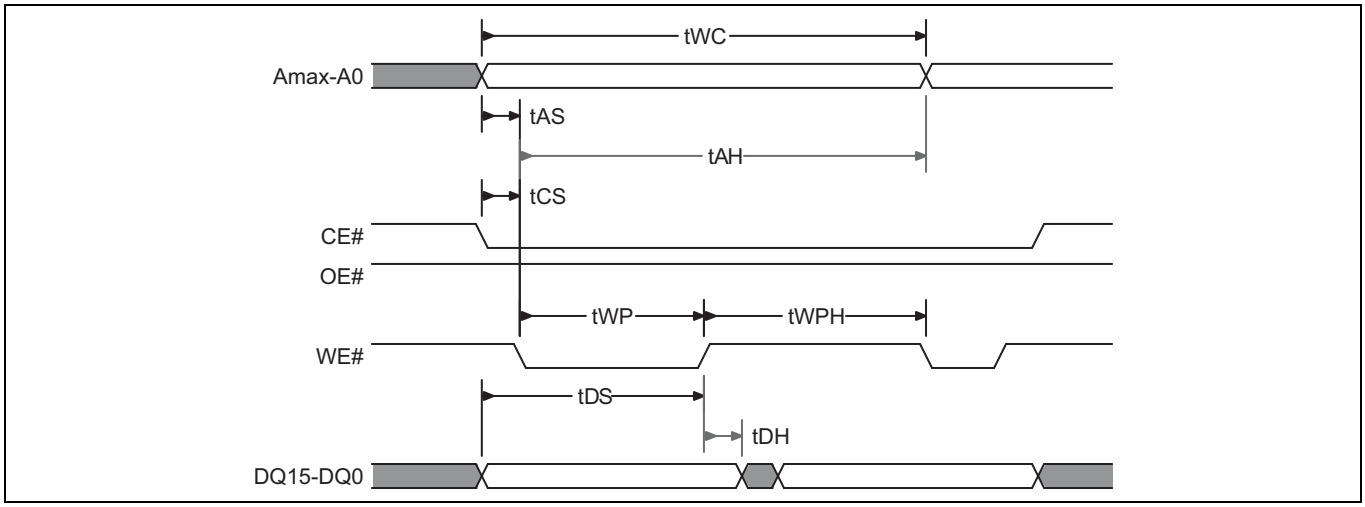


Figure 21 Back to Back (CE#VIL) Write Operation timing diagram

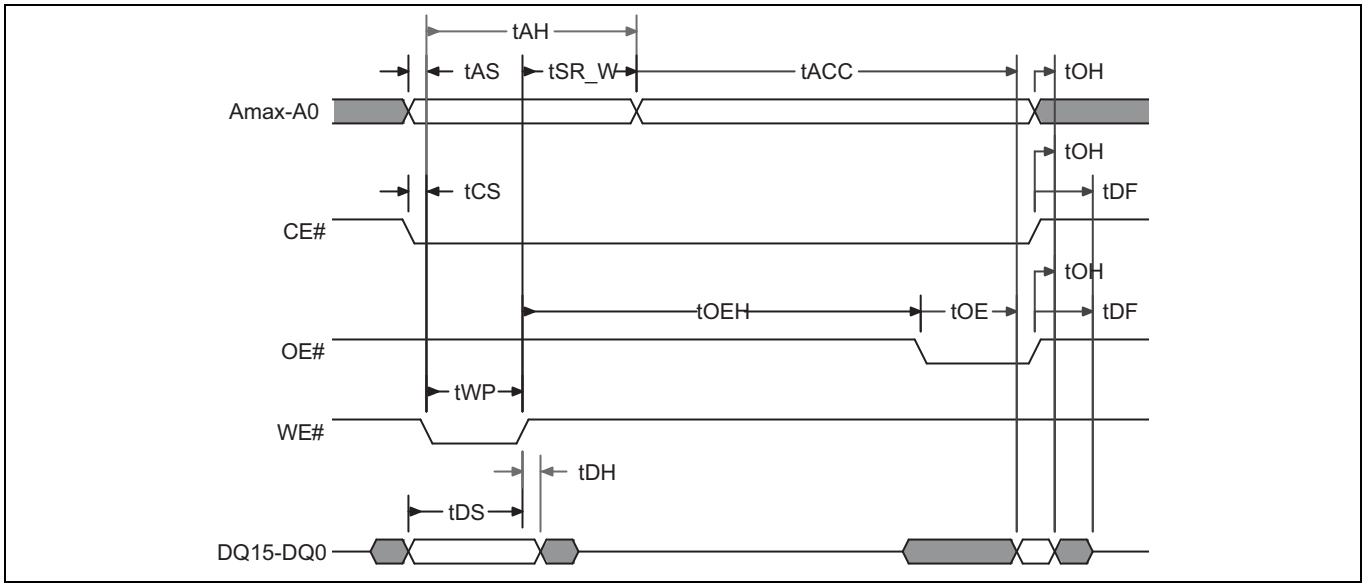


Figure 22 Write to Read (t_{ACC}) Operation timing diagram

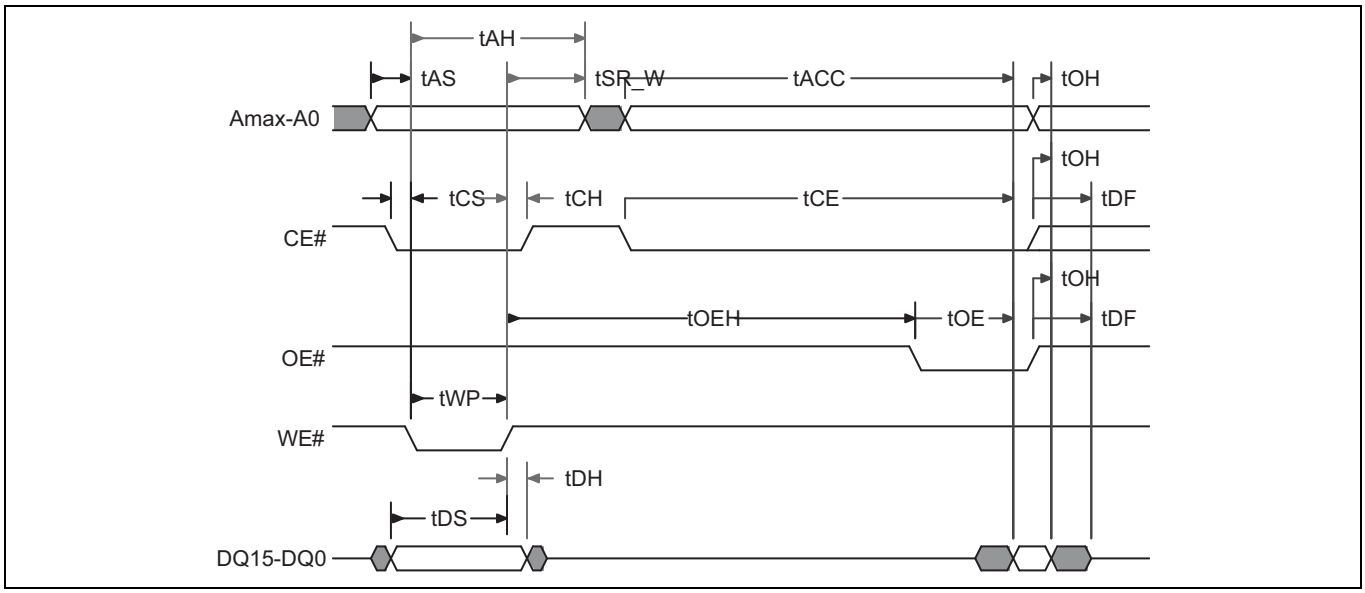


Figure 23 Write to Read (t_{CE}) Operation timing diagram

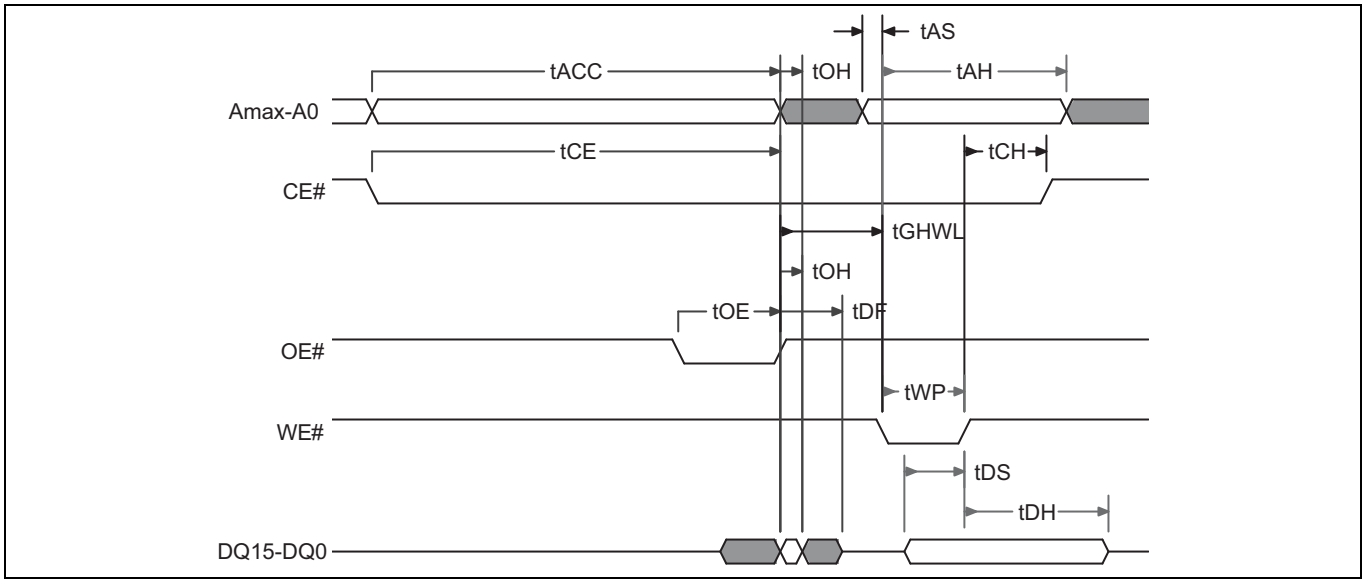


Figure 24 Read to Write (CE# V_{IL}) Operation timing diagram

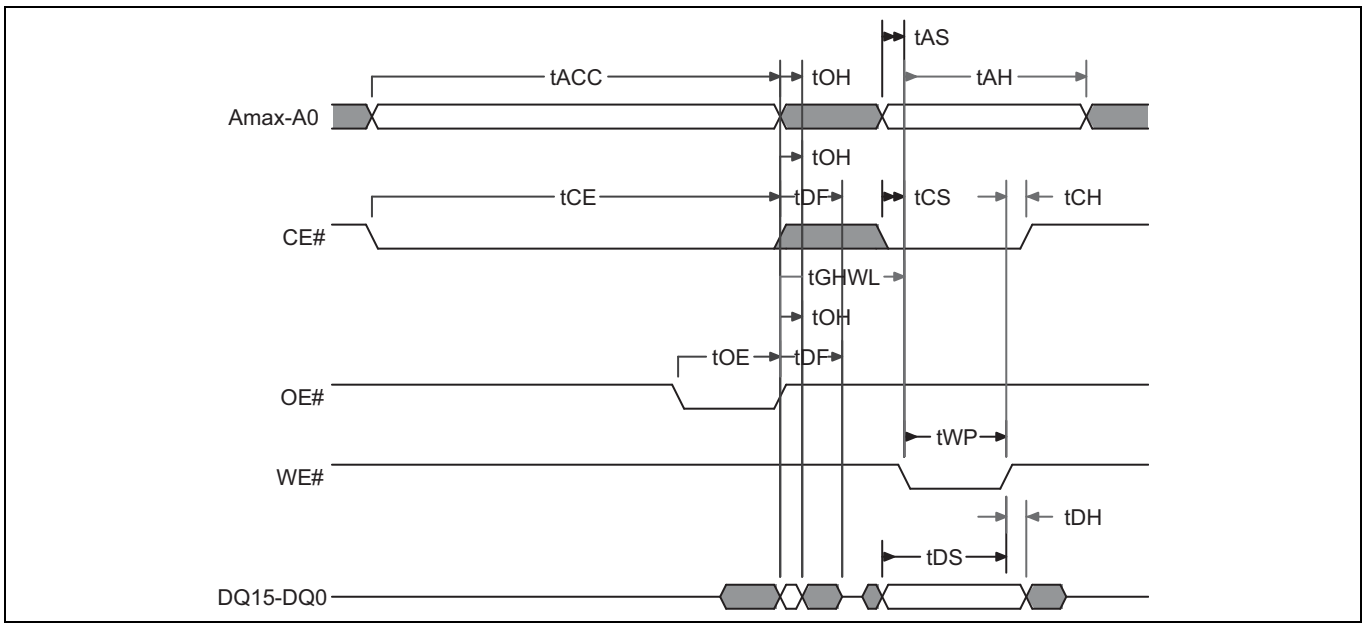


Figure 25 Read to Write (CE# Toggle) Operation timing diagram

Table 68 Erase/Program Operations

Parameter		Description		V_{IO} = 2.7 V to V_{CC}	V_{IO} = 1.65 V to V_{CC}	Unit
JEDEC	Std					
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation	Typ	Note 113		µs
		Effective Write Buffer Program Operation per Word	Typ	Note 113		µs
		Program Operation per Word or Page	Typ	Note 113		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation[114]	Typ	Note 113		ms
	t_{BUSY}	Erase/Program Valid to RY/BY# Delay	Max	80		ns
	$t_{SR/W}$	Latency between Read and Write operations[115]	Min	10		ns
	t_{ESL}	Erase Suspend Latency	Max	Note 113		µs
	t_{PSL}	Program Suspend Latency	Max	Note 113		µs
	t_{RB}	RY/BY# Recovery Time	Min	0		µs

Notes
113. See **Table 16** and **Table 17** for specific values.
114. Not 100% tested.
115. Upon the rising edge of WE#, must wait $t_{SR/W}$ before switching to another address.

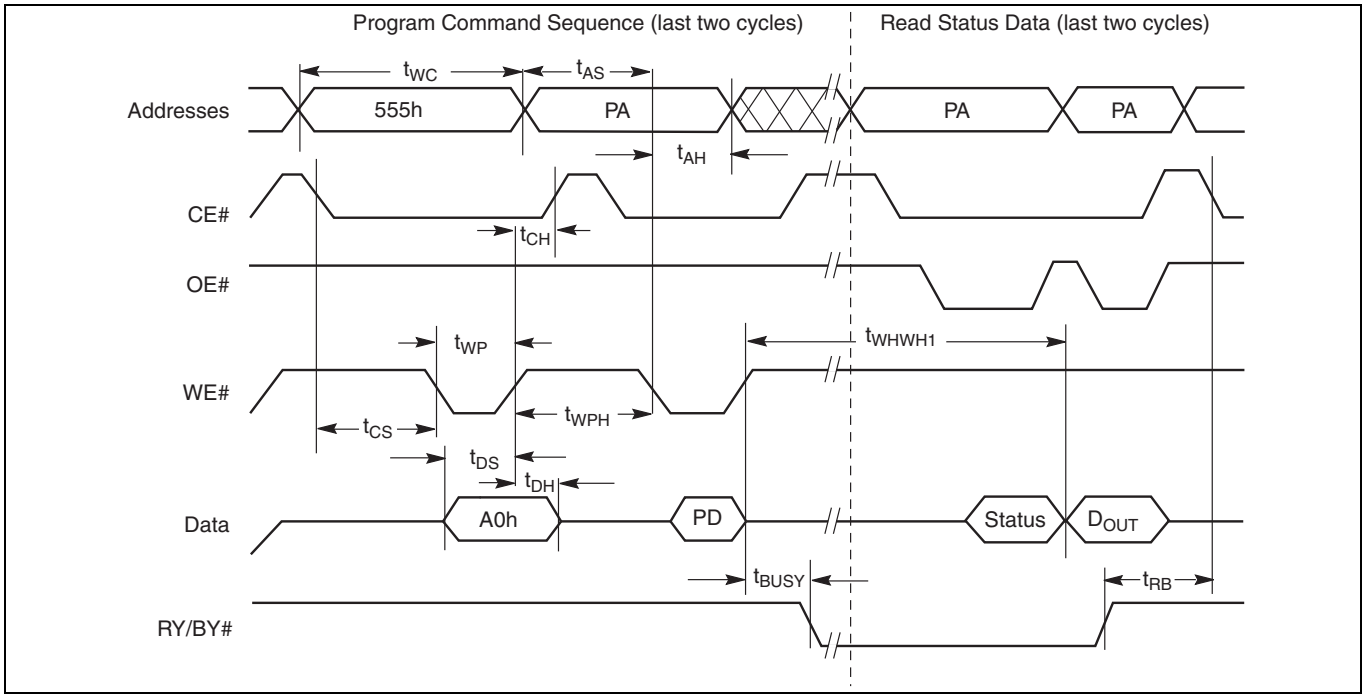


Figure 26 Program Operation timing diagram

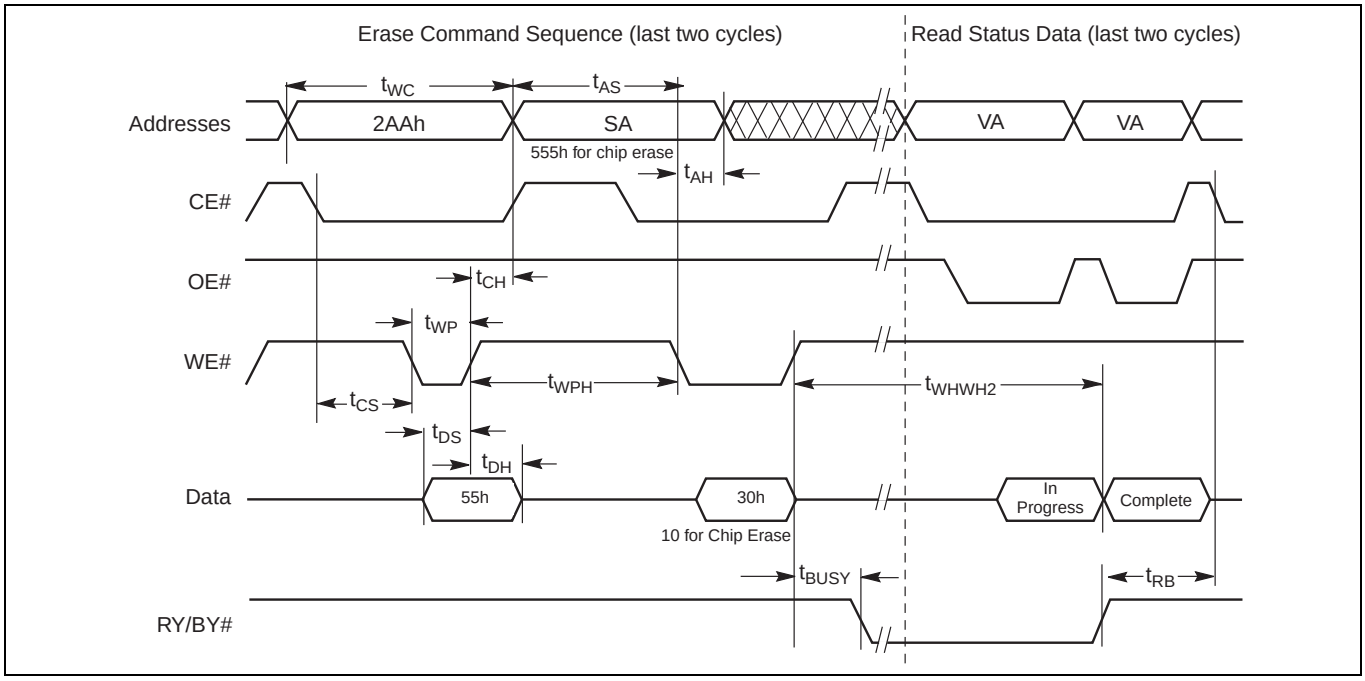


Figure 27 Chip/Sector Erase Operation timing diagram

Notes
116.PA = program address, PD = program data, D_{OUT} is the true data at the program address.
117.SA = sector address (for sector erase), VA = valid address for reading status data.

Table 69 ASO Entry timing

Parameter	Description
$t_{ASOSTART}$	Falling edge of CE# or address change whichever comes last
t_{ASOEND}	Rising edge of CE# or Rising edge of WE# whichever comes first
$t_{ASOENTRY}$	25 ns < $t_{ASOENTRY}$ < 50 ns or $t_{ASOENTRY}$ > 150 ns

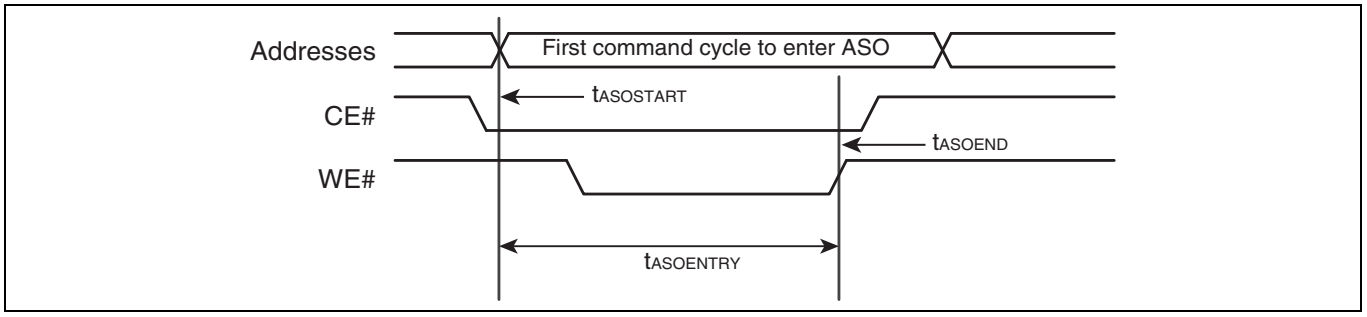


Figure 28 ASO Entry timing

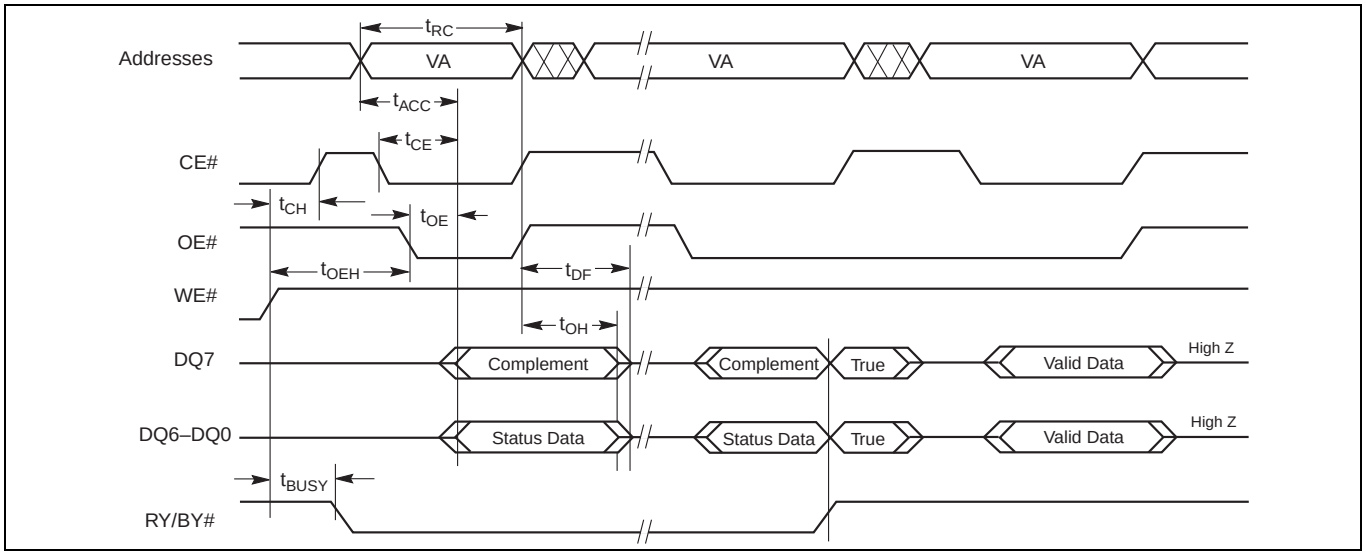


Figure 29 Data# Polling timing diagram (during embedded algorithms)

Notes

118. If this timing cannot be achieved, perform the following steps immediately after ASO Exit and before resuming normal processing: read one word from each of 64 unique 32 byte-aligned pages.
119. Applicable to any ASO entry command.
120. VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

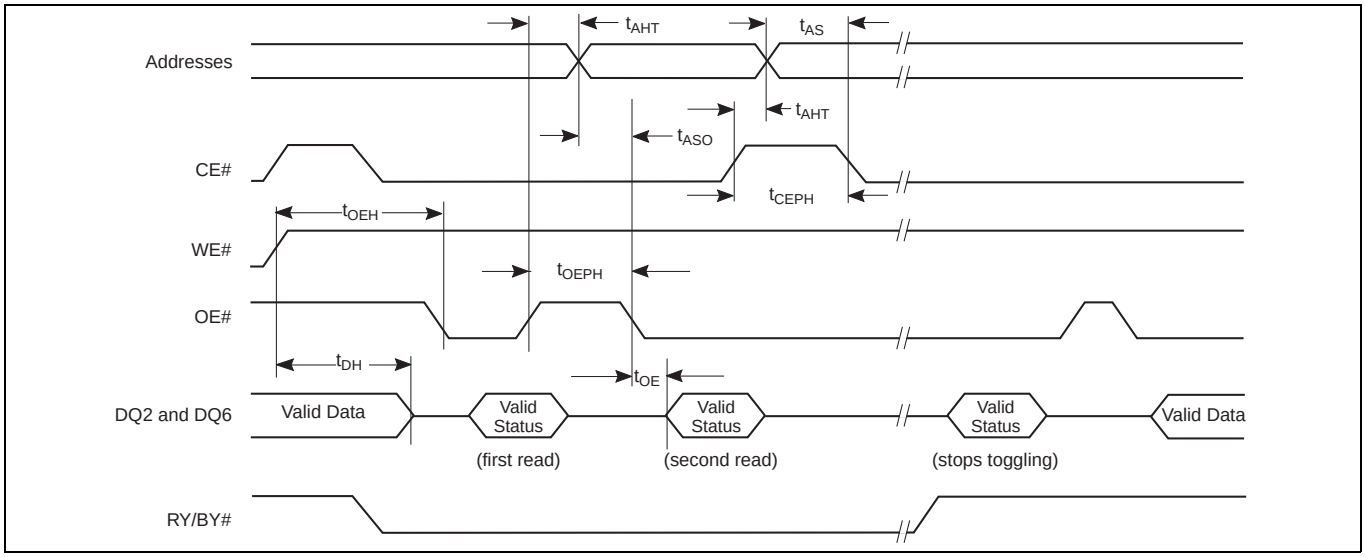


Figure 30 Toggle Bit timing diagram (during embedded algorithms)

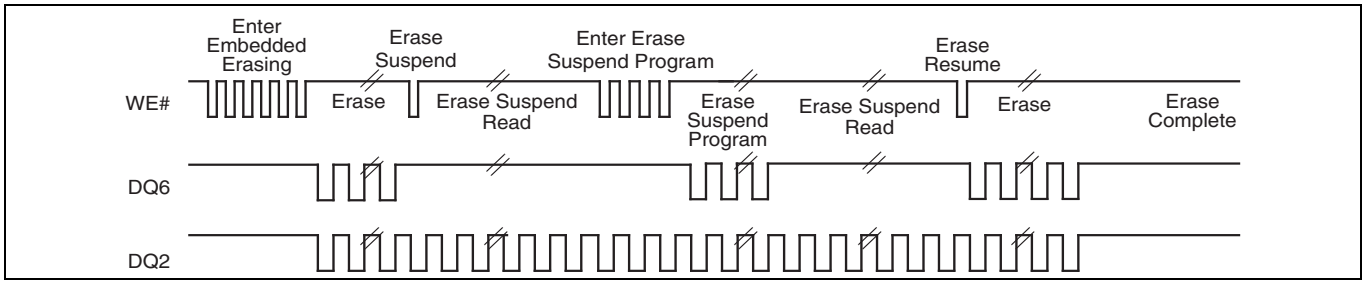


Figure 31 DQ2 vs. DQ6 relationship diagram

Notes

121. DQ6 will toggle at any read address while the device is busy. DQ2 will toggle if the address is within the actively erasing sector.
122. The system may use OE# or CE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within the erase-suspended sector.

11.4.3 Alternate CE# Controlled Write operations

Table 70 Alternate CE# Controlled Write operations

Parameter		Description		V_{IO} = 2.7 V to V_{CC}	V_{IO} = 1.65 V to V_{CC}	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle time[123]	Min	60		ns
t_{AVWL}	t_{AS}	Address Setup time	Min	0		ns
	t_{ASO}	Address Setup time to OE# LOW during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold time	Min	45		ns
	t_{AHT}	Address Hold time From CE# or OE# HIGH during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup time	Min	30		ns
t_{WHDX}	t_{DH}	Data Hold time	Min	0		ns
	t_{CEPH}	CE# HIGH during toggle bit polling	Min	20		ns
	t_{0EPH}	OE# HIGH during toggle bit polling	Min	20		ns
t_{GHEK}	t_{GHEL}	Read Recovery time Before Write (OE# HIGH to WE# LOW)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup time	Min	0		ns
t_{ELWH}	t_{WH}	WE# Hold time	Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	25		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width HIGH	Min	20		ns

Note
123.Not 100% tested.

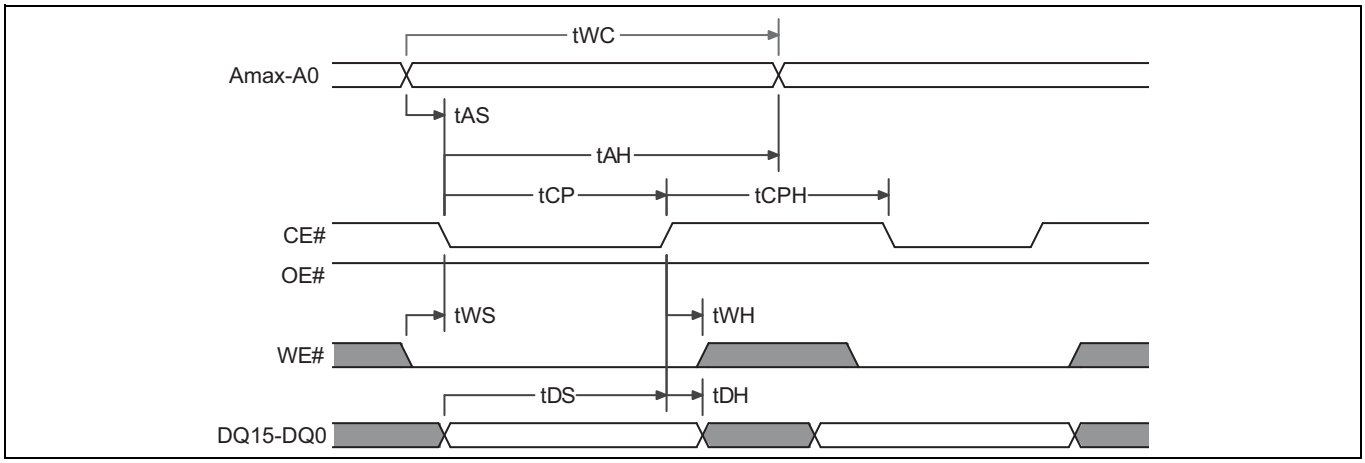


Figure 32 Back to Back (CE#) Write operation timing diagram

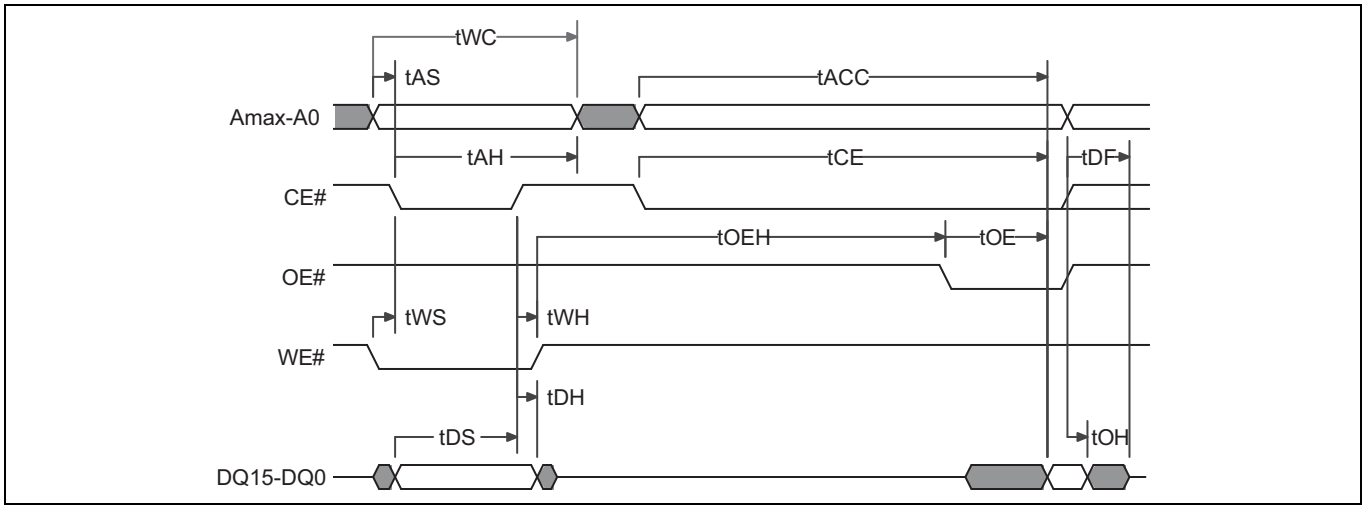


Figure 33 (CE#) Write to Read operation timing diagram

12 Physical interface

12.1 56-pin TSOP

12.1.1 Connection diagram

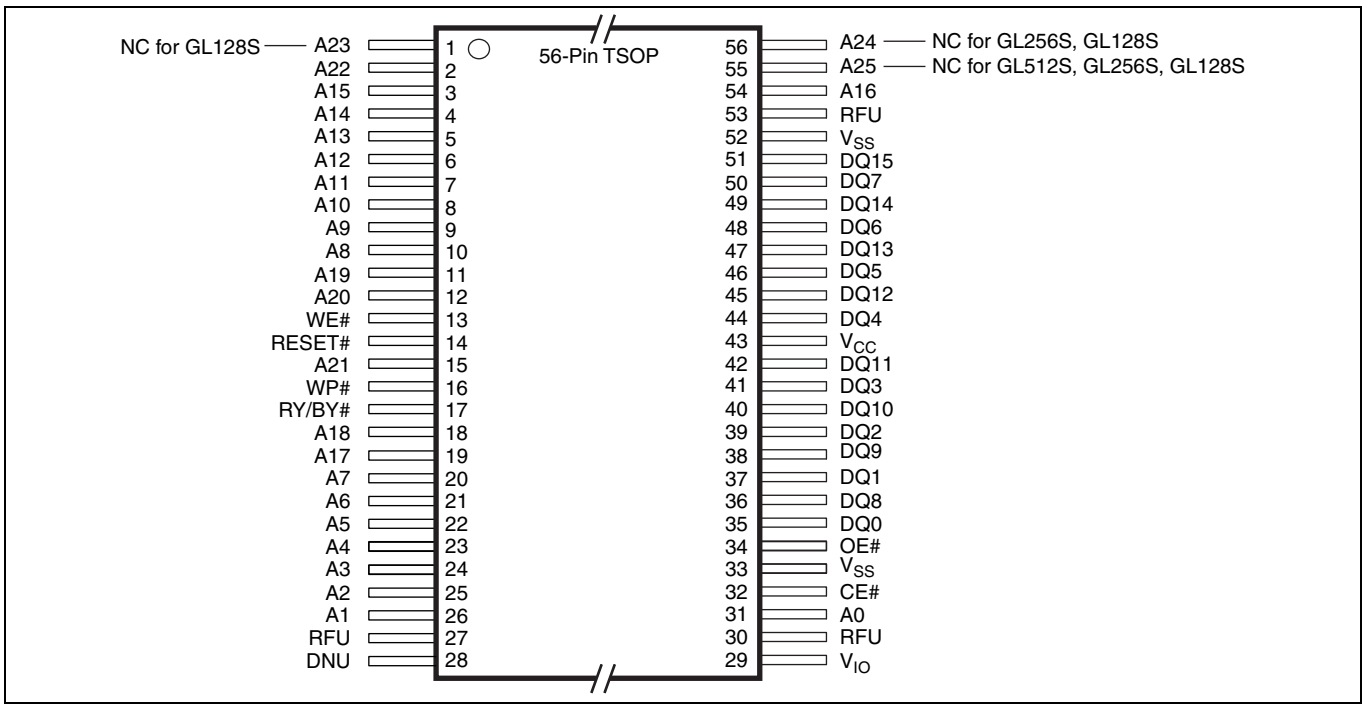
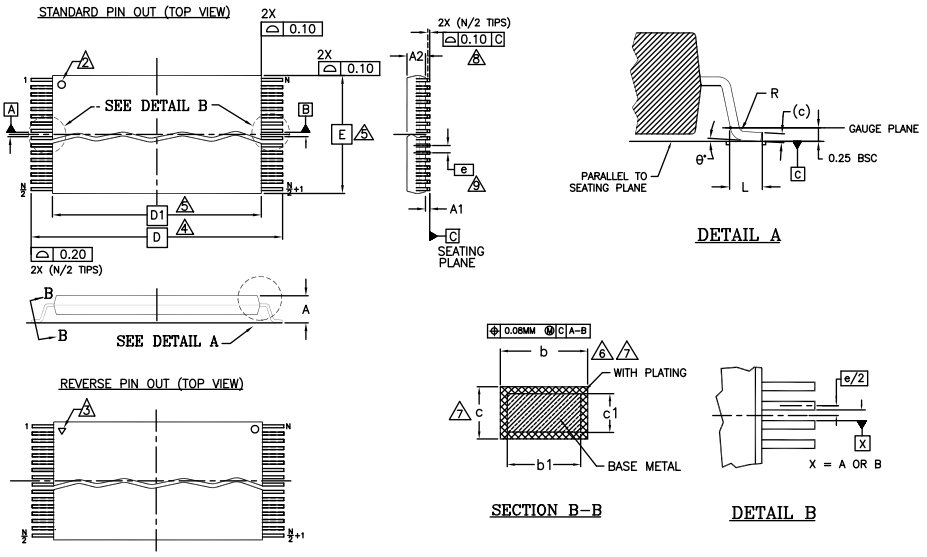


Figure 34 56-pin standard TSOP

Notes

124. Pin 28, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.
125. Pin 27, 30, and 53 Reserved for Future Use (RFU).

12.1.2 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	14.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	56		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)EC.

002-15549 *B

Figure 35 56-pin TSOP (18.4 × 14.0 × 1.2 mm) package outline, 002-15549

12.2 64-ball FBGA

12.2.1 Connection diagram

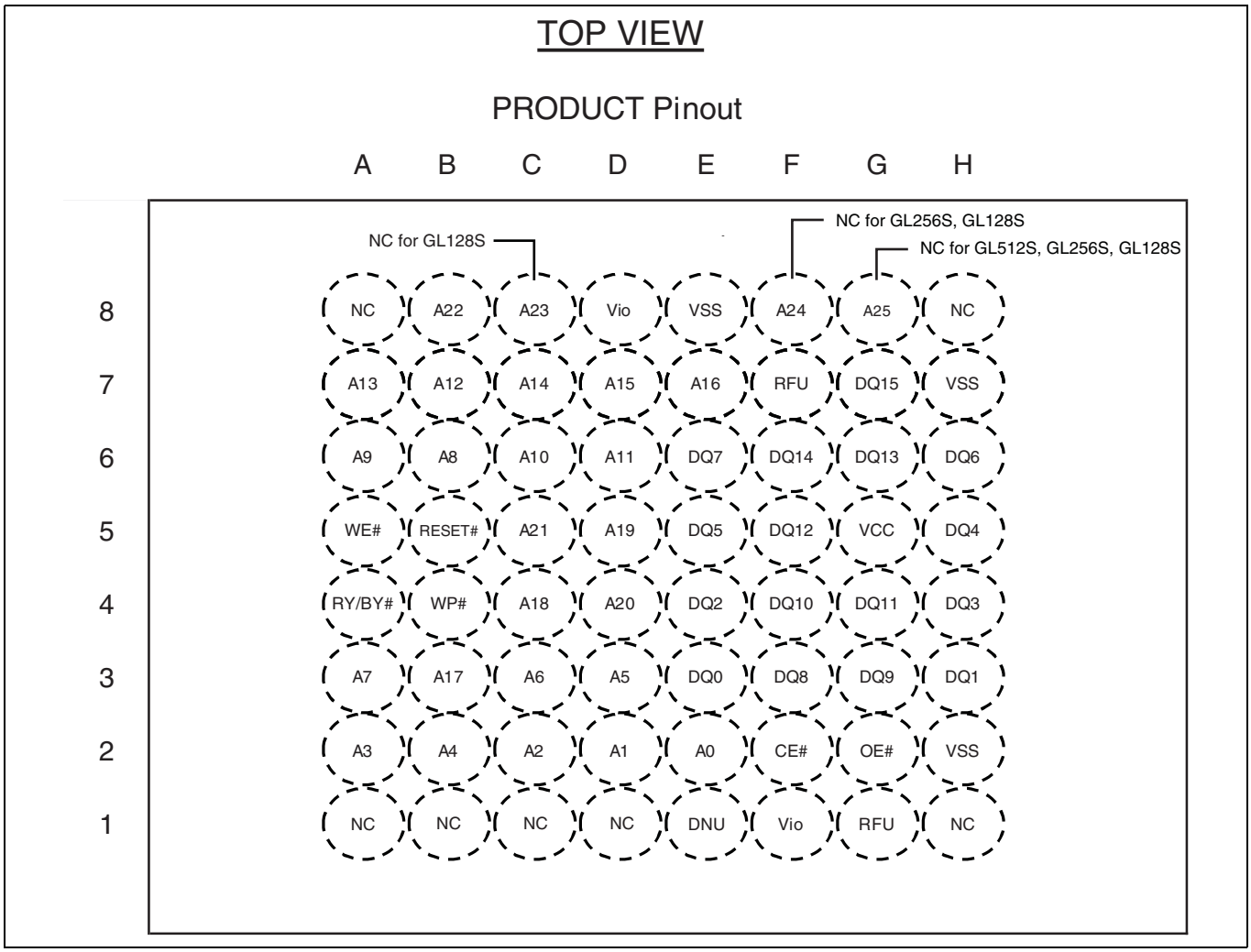
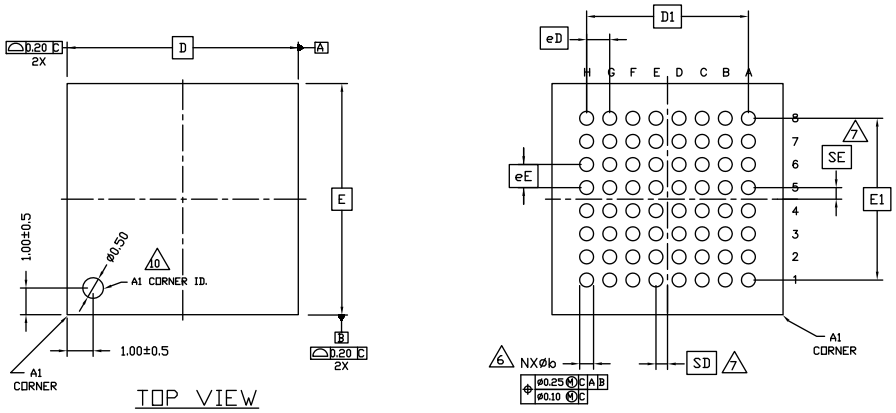


Figure 36 64-ball fortified ball grid array

Notes

126. Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.
127. Balls F7 and G1, Reserved for Future Use (RFU).
128. Balls A1, A8, C1, D1, H1, and H8, No Connect (NC).

12.2.2 Package diagram – LAE064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.40
A1	0.40	-	-
A2	0.60	-	-
D	9.00 BSC.		
E	9.00 BSC.		
D1	7.00 BSC.		
E1	7.00 BSC.		
MD	8		
ME	8		
N	64		
Øb	0.50	0.60	0.70
eD	1.00 BSC.		
eE	1.00 BSC.		
SD/SE	0.50 BSC.		

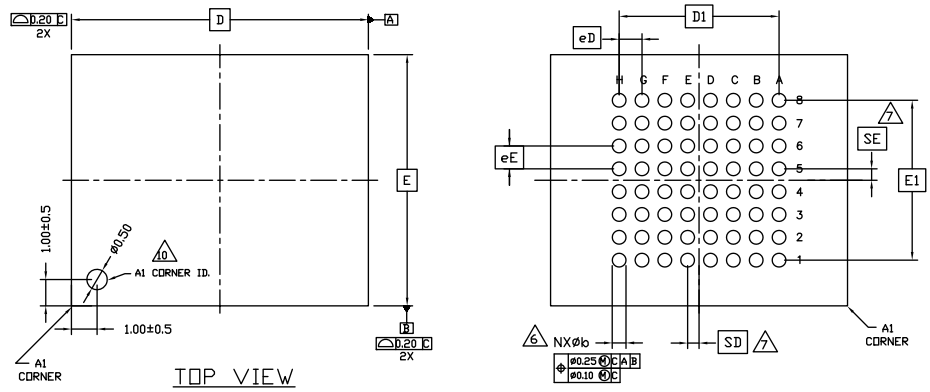
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95 SECTION 3, SPP-020 (RECTANGULAR) OR SPP-010 (SQUARE).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF : N/A

002-15537 *A

Figure 37 64-ball FBGA (9.0 × 9.0 × 1.4 mm) package outline, 002-15537

12.2.3 Package diagram – LAA064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.40
A1	0.40	-	-
A2	0.60	-	-
D	13.00 BSC.		
E	11.00 BSC.		
D1	7.00 BSC.		
E1	7.00 BSC.		
MD	8		
ME	8		
N	64		
Øb	0.50	0.60	0.70
eD	1.00 BSC.		
eE	1.00 BSC.		
SD/SE	0.50 BSC.		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95 SECTION 3, SPP-020 (RECTANGULAR) OR SPP-010 (SQUARE).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15536 **

Figure 38 64-ball FBGA (13.0 × 11.0 × 1.4 mm) package outline, 002-15536

12.3 56-ball FBGA

12.3.1 Connection diagram

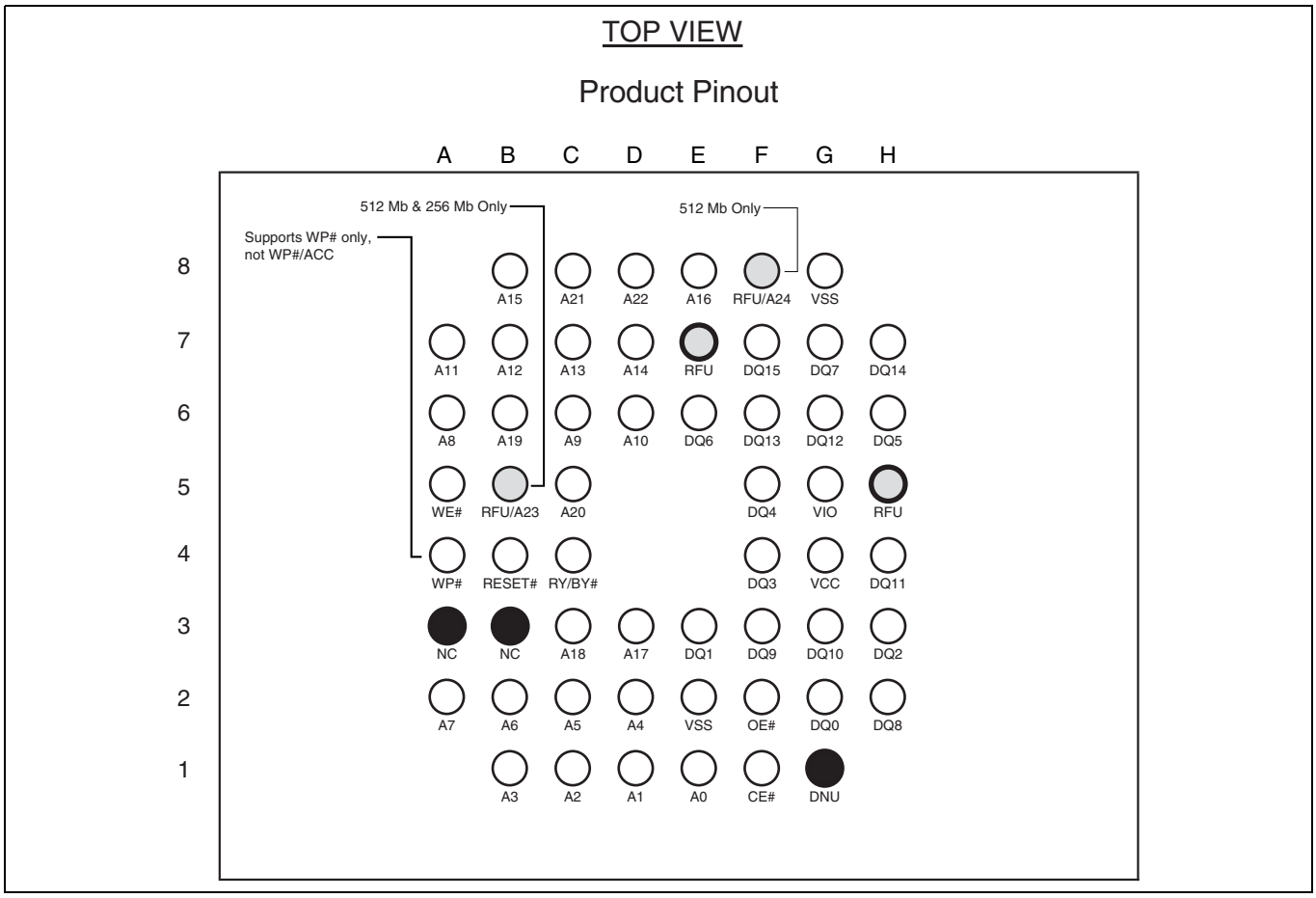
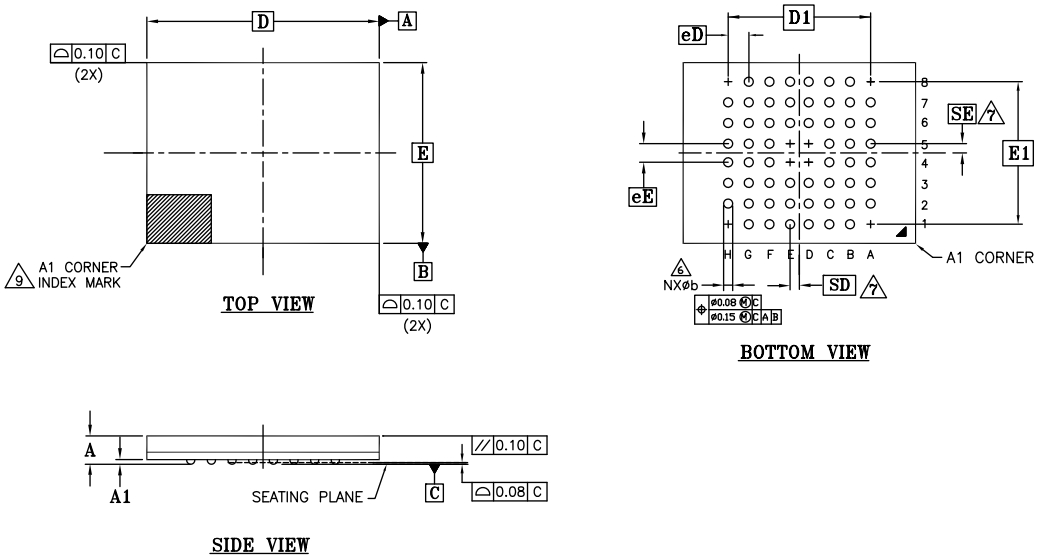


Figure 39 56-ball fortified ball grid array

Notes

129. Ball G1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress® for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.
130. Balls E7, F8, and H5, Reserved for Future Use (RFU).
131. Balls A3 and B3, No Connect (NC).

12.3.2 Package diagram - VBU056



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.17	-	-
D	9.00 BSC.		
E	7.00 BSC.		
D1	5.60 BSC.		
E1	5.60 BSC.		
MD	8		
ME	8		
n	56		
Øb	0.33	-	0.45
eD/eE	0.80 BSC.		
SD/SE	0.40 BSC.		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010/020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE TOTAL NUMBER OF POPULATED SOLDER BALLS FOR MATRIX SIZE MD AND ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 and "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15551 **

Figure 40 56-ball FBGA (9.0 × 7.0 × 1.0 mm) package outline, 002-15551

13 Ordering information

13.1 Ordering code definitions

The ordering part number for the General Market device is formed by a valid combination of the following:

S29GL01GS 10 D H I 01 0

Packing type
0 = Tray
3 = 13” tape and reel

Model number (V_{IO} and V_{CC} range)
01 = V_{IO} = V_{CC} = 2.7 V to 3.6 V, highest address sector protected
02 = V_{IO} = V_{CC} = 2.7 V to 3.6 V, lowest address sector protected
V1 = V_{IO} = 1.65 V to V_{CC}, V_{CC} = 2.7 V to 3.6 V, highest address sector protected
V2 = V_{IO} = 1.65 V to V_{CC}, V_{CC} = 2.7 V to 3.6 V, lowest address sector protected

Temperature range / grade
I = Industrial (–40°C to +85°C)
V = Industrial Plus (–40°C to +105°C)
A = Automotive, AEC-Q100 Grade 3 (–40°C to +85°C)
B = Automotive, AEC-Q100 Grade 2 (–40°C to +105°C)

Package materials set
A = Leaded (Sn/Pb) balls - BGA only
F = Halogen-free, Lead (Pb)-free[132]
H = Halogen-free, Lead (Pb)-free[132]

Package type
D = Fortified ball-grid array package (LAE064) 9 mm x 9 mm
F = Fortified ball-grid array package (LAA064) 13 mm x 11 mm
G = Fortified ball-grid array package (VBU056) 9 mm x 7 mm
S = 70-pin shrink small outline package
T = Thin small outline package (TSOP) standard pinout

Speed option
90 = 90 ns random access time
10 = 100 ns random access time
11 = 110 ns random access time
12 = 120 ns random access time

Device number/description
S29GL01GS, S29GL512S, S29GL256S, S29GL128S
3.0 V Core, with V_{IO} option, 1024, 512, 256, 128 Mb Page-Mode Flash Memory,
Manufactured on 65-nm MIRRORBIT™ Eclipse Process Technology

Note
132.Halogen-free definition is in accordance with IEC 61249-2-21 specification.

13.2 Valid combinations — standard

Table 71 lists the configurations planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Table 71 S29GL-S valid combinations — standard

S29GL-S valid combinations — standard					
Base OPN	**Speed (ns)**	**Package and temperature**	**Model number**	**Packing type**	**Ordering part number (yy = Model number, x = Packing type)**
S29GL01GS	100	DHI, FAI, FHI, TFI[133]	01, 02	0, 3[134]	S29GL01GS10DHIyyx S29GL01GS10FAIyyx S29GL01GS10FHIyyx S29GL01GS10TFIyyx
	110	DHV, TFV[133]	01, 02		S29GL01GS11DHVyyx S29GL01GS11TFVyyx
		DHI, FHI, TFI[133]	V1, V2		S29GL01GS11DHIyyx S29GL01GS11FHIyyx S29GL01GS11TFIyyx
	120	DHV, TFV[133]	V1, V2		S29GL01GS12DHVyyxx S29GL01GS12TFVyyxx
S29GL512S	100	DHI, FAI, FHI, GHI, SFI, TFI[133]	01, 02	0, 3[134]	S29GL512S10DHIyyx S29GL512S10FAIyyx S29GL512S10FHIyyx S29GL512S10GHIyyx S29GL512S10SFIyyx S29GL512S10TFIyyx
	110	GHI[133]	01, 02		S29GL512S11GHIyyx
		DHV, TFV[133]	01, 02		S29GL512S11DHVyyx S29GL512S11TFVyyx
		DHI, FHI, TFI[133]	V1, V2		S29GL512S11DHIyyx S29GL512S11FHIyyx S29GL512S11TFIyyx
	120	DHV, TFV[133]	V1, V2		S29GL512S12DHVyyxx S29GL512S12TFVyyxx
S29GL256S	90	DHI, FHI, GHI, TFI[133]	01, 02	0, 3[134]	S29GL256S90DHIyyx S29GL256S90FHIyyx S29GL256S90GHIyyx S29GL256S90TFIyyx
	100	DHV, TFV[133]	01, 02		S29GL256S10DHVyyx S29GL256S10TFVyyx
		DHI, FAI, FHI, TFI[133]	V1, V2		S29GL256S10DHIyyx S29GL256S10FAIyyx S29GL256S10FHIyyx S29GL256S10TFIyyx
	110	DHV, TFV[133]	V1, V2		S29GL256S11DHVyyxx S29GL256S11TFVyyxx

Table 71 S29GL-S valid combinations — standard (Continued)

S29GL-S valid combinations — standard					
Base OPN	**Speed (ns)**	**Package and temperature**	**Model number**	**Packing type**	**Ordering part number (yy = Model number, x = Packing type)**
S29GL128S	90	DHI, FAI, FHI, GHI, TFI[133]	01, 02	0, 3[134]	S29GL128S90DHIyyx S29GL128S90FAIyyx S29GL128S90FHIyyx S29GL128S90GHIyyx S29GL128S90TFIyyx
	100	DHV, TFV[133]	01, 02		S29GL128S10DHVyyx S29GL128S10TFVyyx
		DHI, FAI, FHI, TFI[133]	V1, V2		S29GL128S10DHIyyx S29GL128S10FAIyyx S29GL128S10FHIyyx S29GL128S10TFIyyx
	110	DHV, TFV, FHV[133]	V1, V2		S29GL128S11DHVyyx S29GL128S11TFVyyx S29GL128S11FHVyyx

Notes
133. Additional speed, package, and temperature options maybe offered in the future. Check with your local sales representative for availability.
134. Package Type 0 is standard option.

13.3 Valid combinations — automotive grade / AEC-Q100

Table 72 and Table 73 list configurations that are automotive grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production part approval process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 72 S29GL-S valid combinations — Automotive grade (–40°C to +85°C)

S29GL-S valid combinations — Automotive grade (–40°C to +85°C)					
Base OPN	**Speed (ns)**	**Package and temperature**	**Model number**	**Packing type**	**Ordering part number (yy = Model number, x = Packing Type)**
S29GL01GS	100,110	DHA, FHA, TFA[135]	01, 02	0, 3[136]	S29GL01GS10DHAyyx S29GL01GS10FHAyyx S29GL01GS10TFAyyx S29GL01GS11DHAyyx S29GL01GS11FHAyyx S29GL01GS11TFAyyx
	110		V1, V2		S29GL01GS11DHAyyx S29GL01GS11FHAyyx S29GL01GS11TFAyyx
S29GL512S	100		01, 02		S29GL512S10DHAyyx S29GL512S10FHAyyx S29GL512S10TFAyyx
	110		V1, V2		S29GL512S11DHAyyx S29GL512S11FHAyyx S29GL512S11TFAyyx
S29GL256S	90		01, 02		S29GL256S90DHAyyx S29GL256S90FHAyyx S29GL256S90TFAyyx
	100		V1, V2		S29GL256S10DHAyyx S29GL256S10FHAyyx S29GL256S10TFAyyx
S29GL128S	90		01, 02		S29GL128S90DHAyyx S29GL128S90FHAyyx S29GL128S90TFAyyx
	100		V1, V2		S29GL128S10DHAyyx S29GL128S10FHAyyx S29GL128S10TFAyyx

Notes

135. Additional speed, package, and temperature options maybe offered in the future. Check with your local sales representative for availability.
136. Package Type 0 is standard option.

Table 73 S29GL-S valid combinations — automotive grade (–40°C to +105°C)

S29GL-S valid combinations — Automotive grade (–40°C to +105°C)					
Base OPN	**Speed (ns)**	**Package and temperature**	**Model number**	**Packing type**	**Ordering part number (yy = Model number, x = Packing Type)**
S29GL01GS	110	DHB, FHB, TFB, GHB[137]	01, 02	0, 3[138]	S29GL01GS11DHByyx S29GL01GS11FHByyx S29GL01GS11TFByyx
	120		V1, V2		S29GL01GS12DHByyx S29GL01GS12FHByyx S29GL01GS12TFByyx
S29GL512S	110		01, 02		S29GL512S11DHByyx S29GL512S11FHByyx S29GL512S11GHByyx S29GL512S11TFByyx
	120		V1, V2		S29GL512S12DHByyx S29GL512S12FHByyx S29GL512S12GHByyx S29GL512S12TFByyx
S29GL256S	100		01, 02		S29GL256S10DHByyx S29GL256S10FHByyx S29GL256S10TFByyx S29GL256S10GHByyx
	110		V1, V2		S29GL256S11DHByyx S29GL256S11FHByyx S29GL256S11TFByyx
S29GL128S	100		01, 02		S29GL128S10DHByyx S29GL128S10FHByyx S29GL128S10TFByyx S29GL128S10GHByyx
	110		V1, V2		S29GL128S11DHByyx S29GL128S11FHByyx S29GL128S11TFByyx

Notes
137. Additional speed, package, and temperature options maybe offered in the future. Check with your local sales representative for availability.
138. Package Type 0 is standard option.

Revision history

Document revision	Date	Description of changes
**	2011-02-11	Initial release.
*A	2011-03-21	**Global:** Modified document from “Advance Information” to “Preliminary” **OPN:** Added FBGA package offering for V1 & V2 Model Number Removed KGD information, which is documented in a separate Supplement **Command Definitions Table:** Removed duplicated commands Changed the number of command cycles for a CFI Enter from 3 to 1 **Physical Interface:** Updated 56-pin TSOP pinout figure Updated 64-ball FBGA pinout figure **Other Resources:** Added additional application notes in “Links to Application Notes” **Lock Register Table:** Changed the default value of bit 7 in the Lock register
*B	2011-07-08	**Performance Summary:** Updated table: Typical Program and Erase Rates **Secure Silicon Region ASO:** Corrected table: Secure Silicon Region **DQ1: Write-to-Buffer Abort:** Corrected table: Data Polling Status **Embedded Algorithm Performance Table:** Updated table: Embedded Algorithm Characteristics Command State Transitions: Corrected tables: changed Software Reset/ASO Exit Data value to from 00F0h to xF0h Corrected table: Erase Suspend Unlock State Command Transition Corrected table: Erase Suspend - DYB State Command Transition Corrected table: Program Unlock State Command Transition Corrected table: Lock Register State Command Transition Corrected table: Secure Silicon Sector Program State Command Transition Corrected table: Password Protection Command State Transition Corrected table: Non-Volatile Protection Command State Transition Corrected table: PPB Lock Bit Command State Transition Corrected table: Volatile Sector Protection Command State Transition Device ID and Common Flash Interface (ID-CFI) ASO Map: Corrected table: Corrected CFI Primary Vendor-Specific Extended Query description for Word Address (SA) + 0045h

Revision history

Document revision	Date	Description of changes
*B	2011-07-08	**DC Characteristics:** Updated VIL Max Updated Note **Power-On Reset (POR) and Warm Reset:** Updated table: added row to bottom of table Power-On (Cold) Reset (POR): Updated text Updated figure: Power-Up Diagram **Hardware (Warm) Reset:** Updated figure: Hardware Reset Asynchronous Write Operations: Added figure: Back to Back (CE#VIL) Write Operation Timing Diagram Updated table: Erase/Program Operations **Physical Diagram - LAA064:** Added figure
*C	2011-10-03	**Power-Up Write Inhibit:** Minor correction **PPB Password Protection Mode:** Minor correction **Embedded Algorithm Characteristics table:** Updated Buffer Programming Time maximum limits **Absolute Maximum Ratings table:** Added clarification **DC Characteristics table:** Output High Voltage clarification **Power-Up/Power-Down Voltage and Timing table:** Added clarification **Power-Up figure:** Added clarification **Power-On (Cold) Reset (POR):** Added clarification **Valid Combinations table:** Updated table
*D	2011-12-14	**Global:** Data sheet designation changed from Preliminary to Full Production **Sector Erase:** Updated Typical Erase Time **Capacitance Characteristics:** Updated section **Ordering Information:** Corrected note designation in valid combination table
*E	2012-03-16	**Global:** Added 9 mm x 7 mm package Added 105°C offering **Ordering Information:** Updated Valid Combinations

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*F	2012-12-21	**Distinctive Characteristics:** Added In-Cabin temperature range **Status Register ASO:** Added clarification **Advanced Sector Protection Overview:** Updated figure **PPB Lock:** Added clarification **Persistent Protection Bits (PPB):** Added clarification **Dynamic Protection Bits (DYB):** Added clarification PPB Password Protection Mode: Added clarification **Chip Erase:** Added clarification **Sector Erase:** Added clarification **Erase Suspend / Erase Resume:** Added clarification **Status Register ASO:** Added clarification **Status Register:** Added clarification **DQ7: Data# Polling:** Added clarification **DQ1: Write-to-Buffer Abort:** Added clarification **Data Polling Status:** Updated table **Embedded Operation Error:** Added clarification **Protection Error:** Added clarification **Write Buffer Abort:** Added clarification **Performance Table:** Updated Embedded Algorithm Characteristics (-40°C to +105°C) table Device ID and Common Flash Interface (ID-CFI) ASO Map: Updated CFI Device Geometry Definition table Updated CFI Primary Vendor-Specific Extended Query table Asynchronous Read Operations: Added Read Operation VIO = 1.65 (–40°C to +105°C) table Asynchronous Write Operations: Updated Read to Write (CE# VIL) figure Updated Read to Write (CE# Toggle) figure
*G	2013-10-09	**S29GL-S Valid Combinations Table:** Added VIO Models for Automotive In Cabin Temperature Range
*H	2015-08-13	Updated to Cypress template.

Revision history

Document revision	Date	Description of changes
*I	2016-03-04	Updated **"Ordering information"** on page 107: Updated **Table 71**: Updated part numbers. Replaced "In Cabin" with "Industrial Plus" in Ordering Code Definitions below **Table 71**. Updated to new template.
*J	2016-09-06	Updated **"Timing specifications"** on page 81: Updated **"AC characteristics"** on page 85: Updated **"Asynchronous Write Operations"** on page 90: Updated **Table 69**. Updated **Figure 28**.
*K	2016-11-10	Added Automotive Grade related information in all instances across the document. Updated **"Address space maps"** on page 7: Added **"ECC status ASO"** on page 13. Updated **"Embedded operations"** on page 21: Added **"Automatic ECC"** on page 23. Updated **"Command set"** on page 24: Added **"ECC Status ASO"** on page 35. Updated **"Data integrity"** on page 57: Added **"Erase endurance"** on page 57. Added **"Data retention"** on page 57. Updated **"Software interface reference"** on page 58: Removed "Address and Data Configuration". Updated **"Command summary"** on page 58: Updated **Table 41** (to include ECC ASO Commands). Updated **"Electrical specifications"** on page 74: Added **"Thermal resistance"** on page 74. Updated **"Ordering information"** on page 107: Added **"Valid combinations — automotive grade / AEC-Q100"** on page 110. Updated **"Other resources"** on page 113: Added **"Cypress Flash Memory Roadmap"** on page 113. Updated **"Links to software"** on page 113: Updated description. Updated **"Links to Application Notes"** on page 113: Updated description. Removed "Specification Bulletins". Removed "Contacting Cypress".
*L	2017-05-03	Updated **"Software interface reference"** on page 58: Added **"Device ID and Common Flash Interface (ID-CFI) ASO Map"** on page 67. Updated **"Ordering information"** on page 107: Updated **"Valid combinations — standard"** on page 108: Updated **Table 71**: Updated part numbers. Updated to new template.
*M	2017-06-16	Updated **"Software interface reference"** on page 58: Updated **"Command summary"** on page 58: Updated **Table 41**: Replaced "2" with "1" in "Cycles" column corresponding to "Command Set Exit" under "ECC ASO" Command Sequence.

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*N	2017-07-21	Updated **"Address space maps"** on page 7: Updated **"ECC status ASO"** on page 13: Updated description. Updated **"ECC status"** on page 13: Updated description. Updated **Table 10** (Updated "Name" corresponding to Bit 2 and Bit 1). Updated **"Embedded operations"** on page 21: Updated **"Command set"** on page 24: Updated **"ASO Entry and Exit"** on page 33: Updated **"ECC Status ASO"** on page 35: Updated description. Completing Sunset Review.
*O	2017-09-19	Updated **"Ordering information"** on page 107: Updated **"Valid combinations — standard"** on page 108: Updated **Table 71**: Updated part numbers.
*P	2018-03-30	Updated **"Ordering information"** on page 107: Updated **"Valid combinations — standard"** on page 108: Updated **Table 71**: Updated part numbers. Updated **"Valid combinations — automotive grade / AEC-Q100"** on page 110: Updated **Table 73**: Updated part numbers. Updated to new template.
*Q	2018-06-06	Updated **"Electrical specifications"** on page 74: Updated **"Thermal resistance"** on page 74: Updated **Table 51**: Changed value of Theta Ja parameter from 20.4 °C/W to 27.3 °C/W corresponding to "LAE064" package.
*R	2018-06-21	Updated **"Ordering information"** on page 107: Updated details corresponding to "F" and "H" under "Package Materials Set" in the diagram. Added a note "Halogen free definition is in accordance with IEC 61249-2-21 specification" and referred the same note in "F" and "H".
*S	2022-10-28	Updated Document Title to read as "S29GL01GS, S29GL512S, S29GL256S, S29GL128S, 128 Mb / 256 Mb / 512 Mb / 1 Gb GL-S MIRRORBIT™ Flash Parallel, 3.0 V". Removed "Software Interface". Updated **"Address space maps"** on page 7: Updated **"Device ID and common flash interface (ID-CFI) ASO map — automotive only"** on page 10: Updated **"Common flash memory interface"** on page 11: Updated description. Updated **"Embedded operations"** on page 21: Updated **"Command set"** on page 24: Updated **"ASO Entry and Exit"** on page 33: Updated **"ID-CFI ASO"** on page 33: Updated description.

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Document revision	Date	Description of changes
*S (cont.)	2022-10-28	Updated **“Data integrity”** on page 57: Updated **“Data retention”** on page 57: Updated description. Updated hyperlinks. Removed “Hardware Interface”. Updated **“Electrical specifications”** on page 74: Updated **“Thermal resistance”** on page 74: Updated **Table 51**. Updated **“Physical interface”** on page 100: Updated **“56-pin TSOP”** on page 100: Updated **“Package diagram”** on page 101: Replaced existing spec with 002-15549 *B. Updated **“64-ball FBGA”** on page 102: Updated **“Package diagram – LAE064”** on page 103: Replaced existing spec with 002-15537 *A. Updated **“Package diagram – LAE064”** on page 103: Replaced existing spec with 002-15536 **. Updated **“56-ball FBGA”** on page 105: Updated **“Package diagram - VBU056”** on page 106: Replaced existing spec with 002-15551 **. Removed “Special handling instructions for FBGA package”. Removed “Other resources”. Migrated to Infineon template.

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